

Основи рачунарске технике 2

Испит – Л4

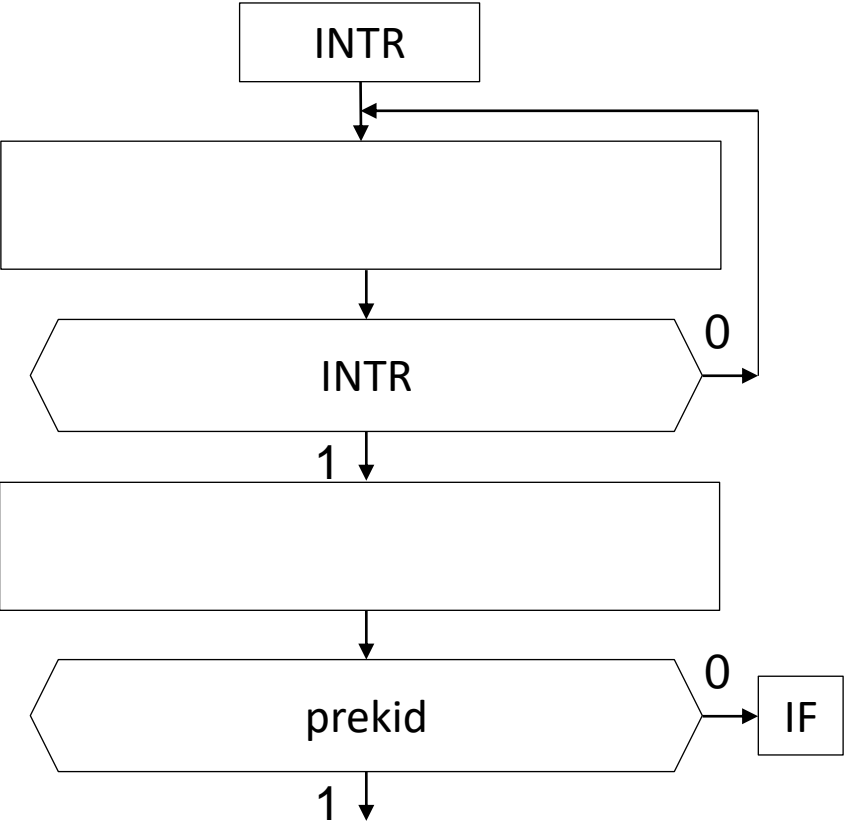
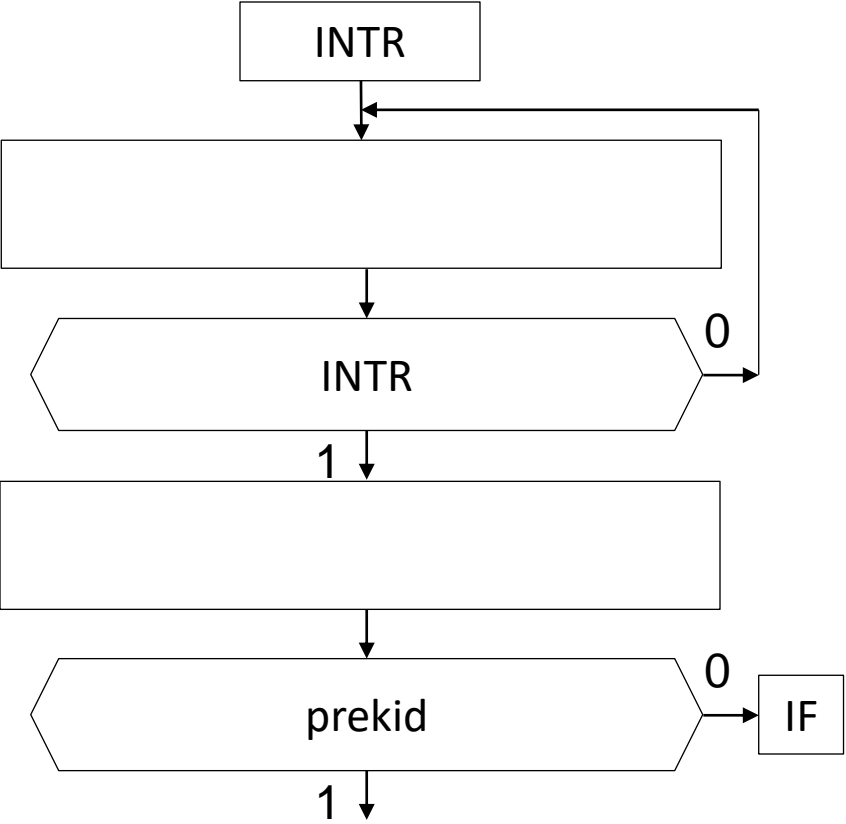
Основи рачунарске технике 2

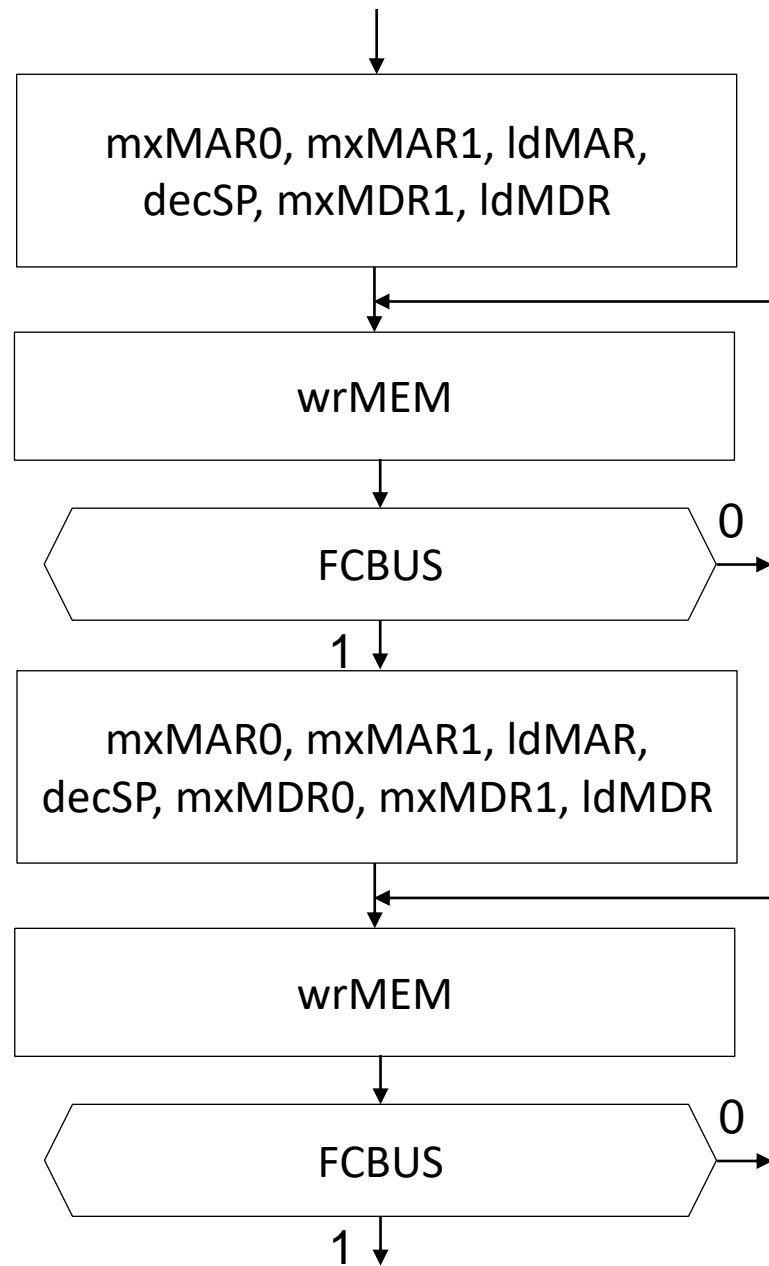
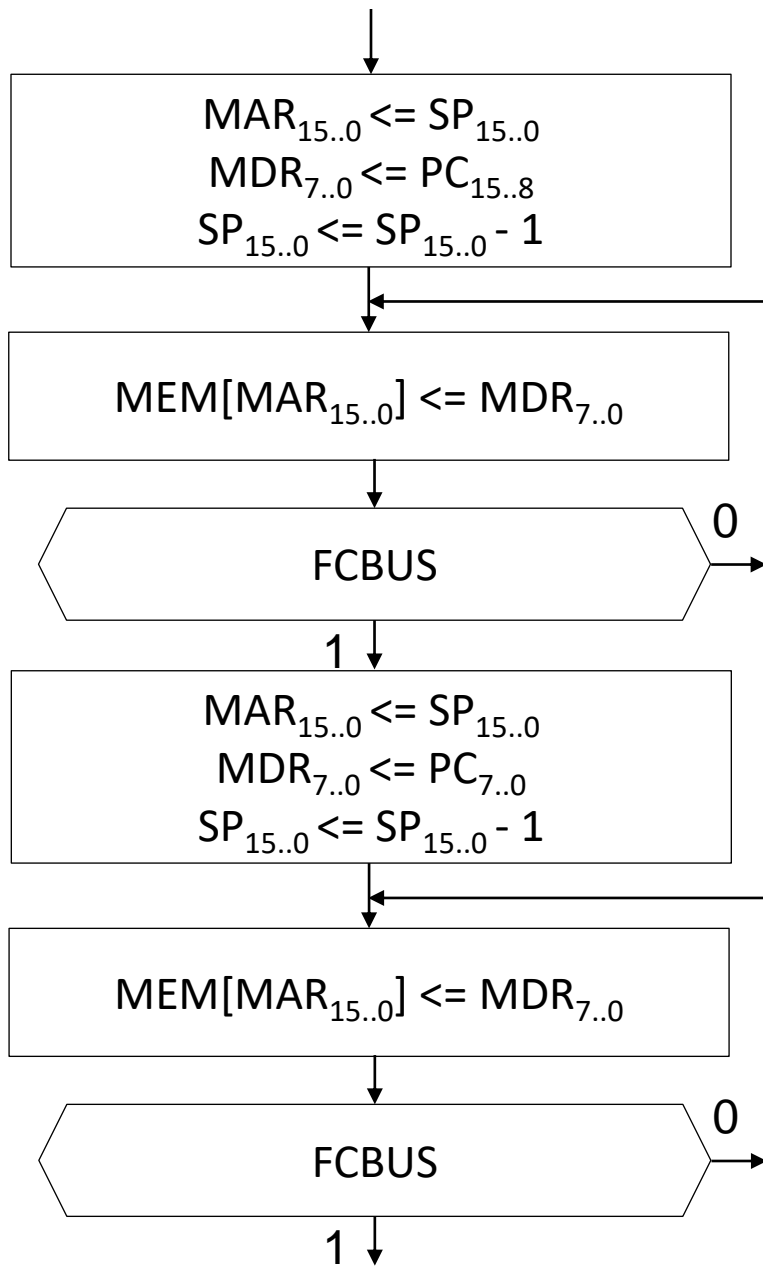
INTR блок

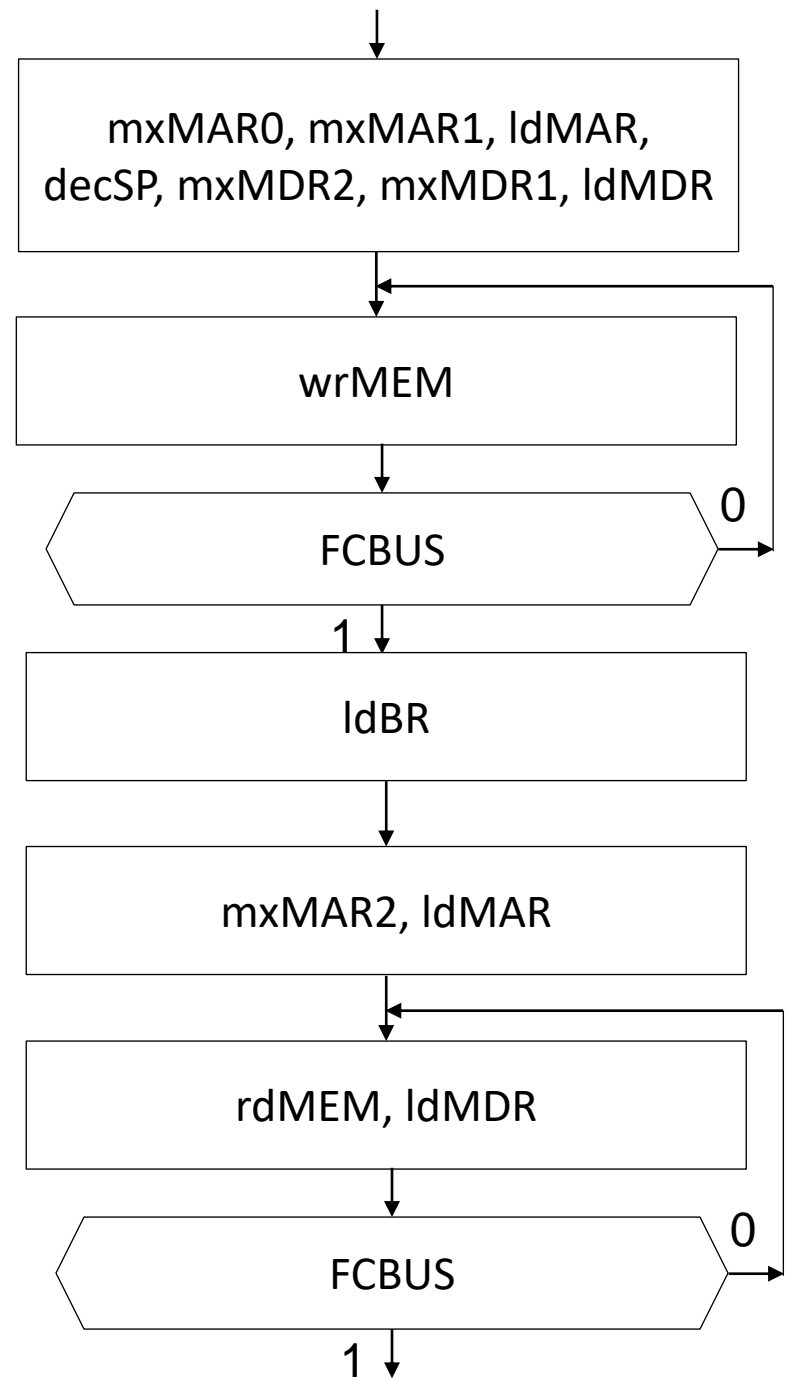
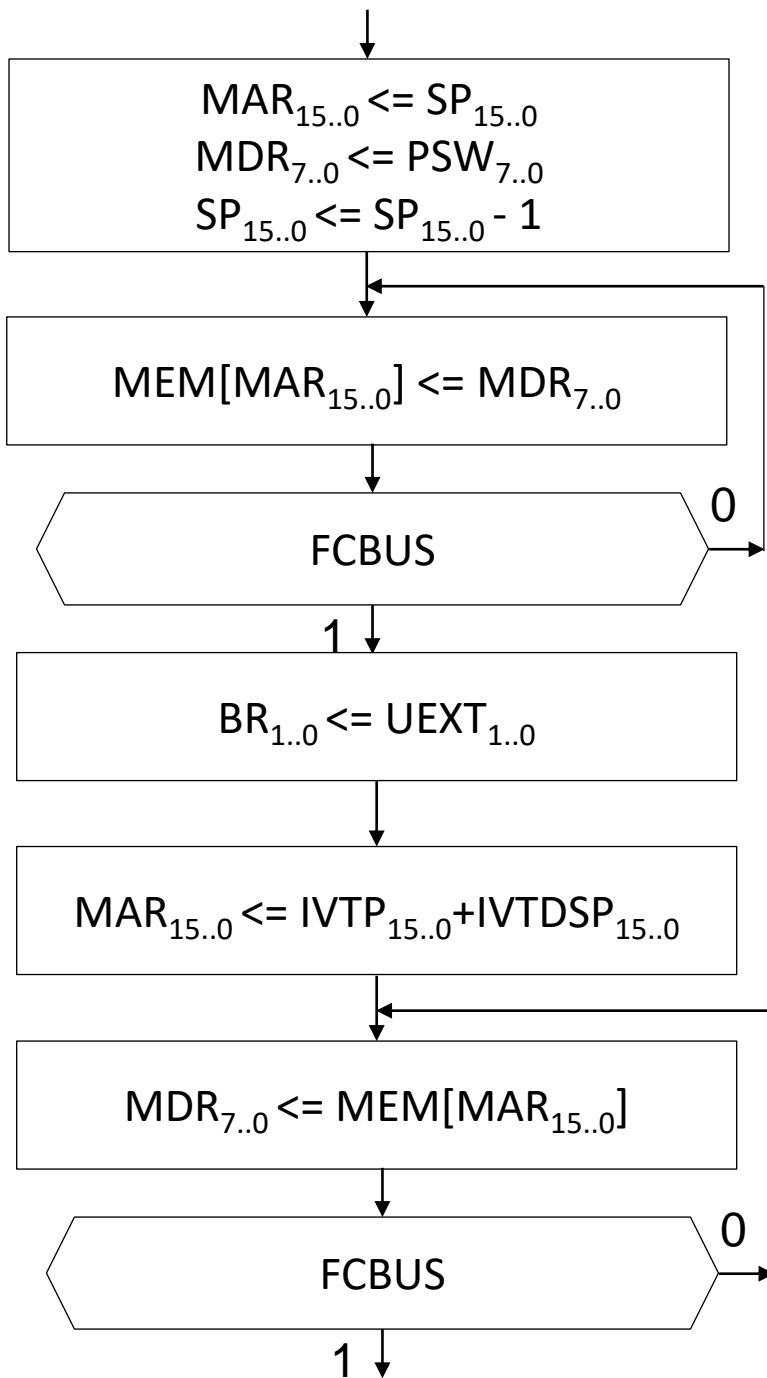
Инструкција	IR _{23..19}	Инструкција	IR _{23..16}	IR _{15..8}	IR _{7..0}	Дужина
LD	0011 0b	JSR	0010 0001b	млађи бајт	старији бајт	3B
ST	0011 1b	JMP	0010 0000b	млађи бајт	старији бајт	3B
ADD	0100 0b	JLEQ	0001 0010b	млађи бајт	старији бајт	3B
SUB	0100 1b	BGREU	0001 0001b	померај	/	2B
		BLSS	0001 0000b	померај	/	2B
		POPGPR	0000 0100b	/	/	1B
		PUSHGPR	0000 0011b	/	/	1B
		RTI	0000 0010b	/	/	1B
		RTS	0000 0001b	/	/	1B
		HALT	0000 0000b	/	/	1B

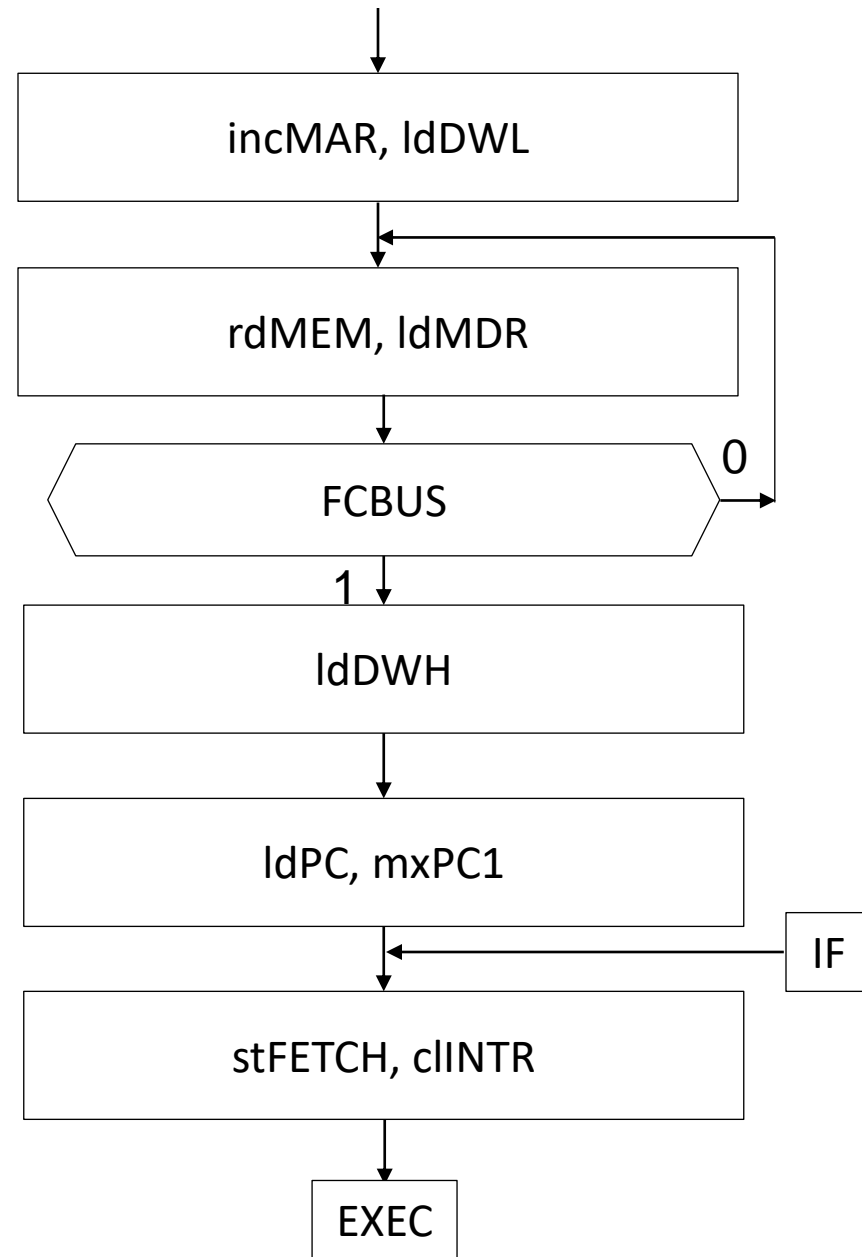
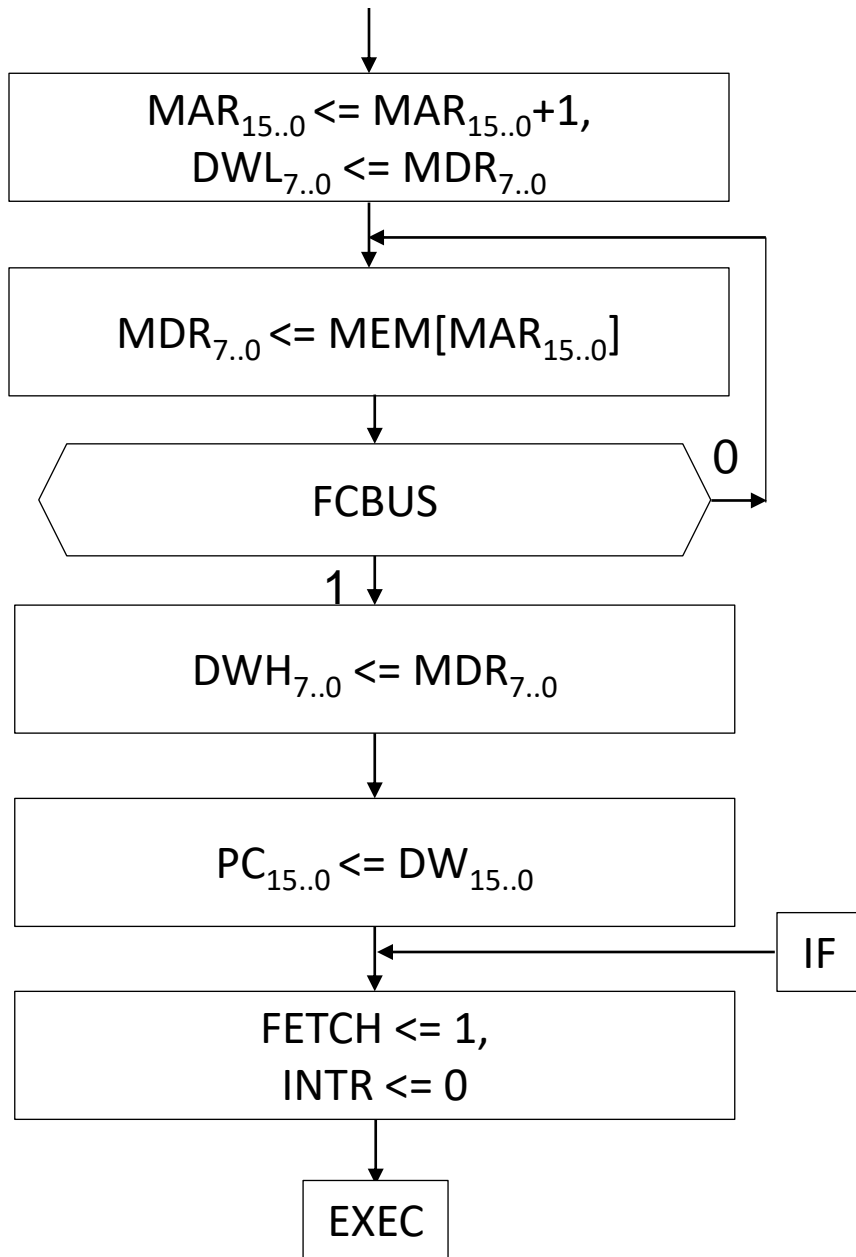
Адресирања	IR _{18..16}	IR _{15..8}	IR _{7..0}	Дужина
regindpom	011b	PPPP PRRRb	/	2B
regdir	010b	XXXX XRRRb	/	2B
memdir	001b	млађи бајт	старији бајт	3B
immed	000b	податак	/	2B

	Нижа адреса	Виша адреса
Адреса	млађи	старији

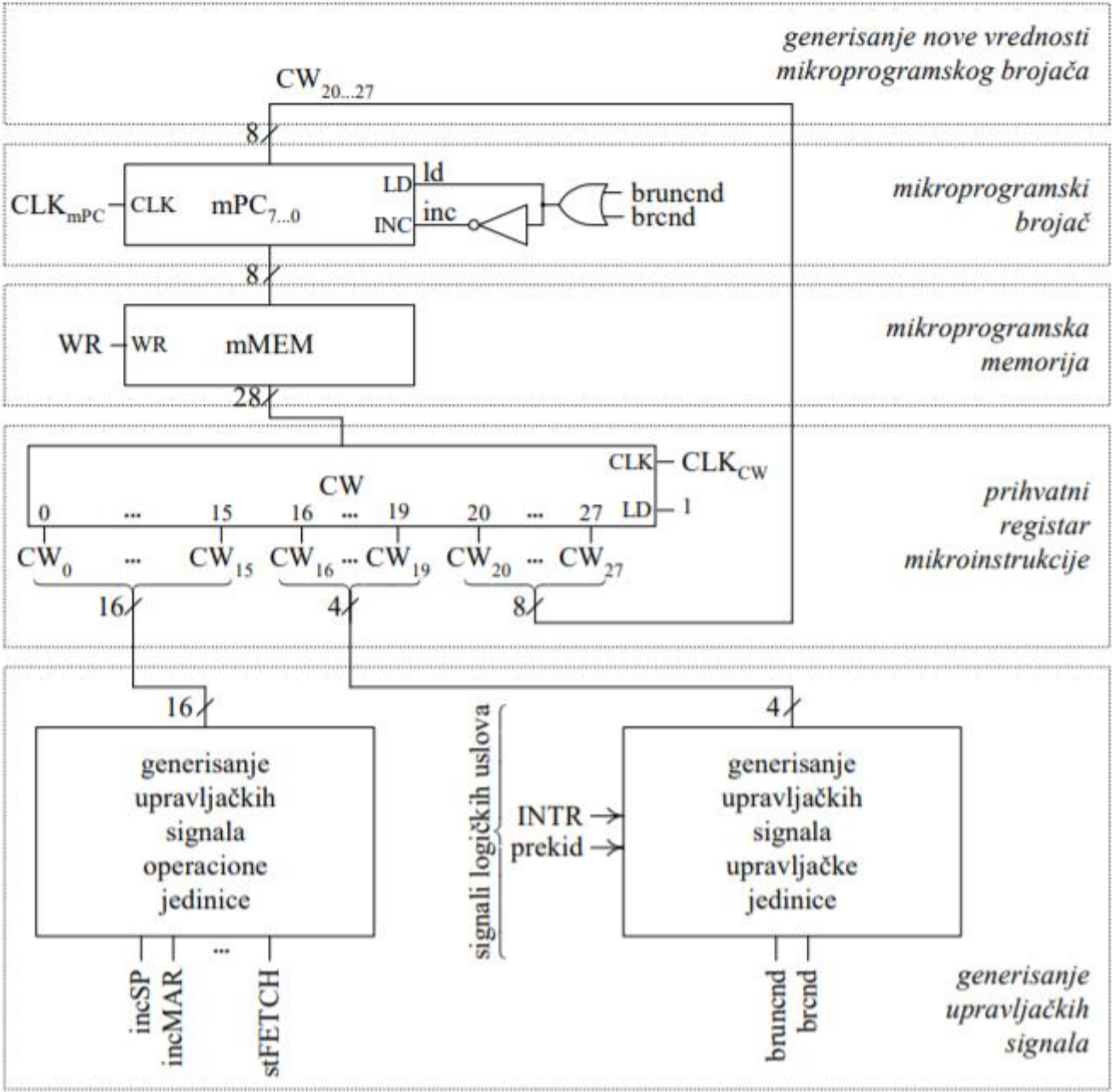




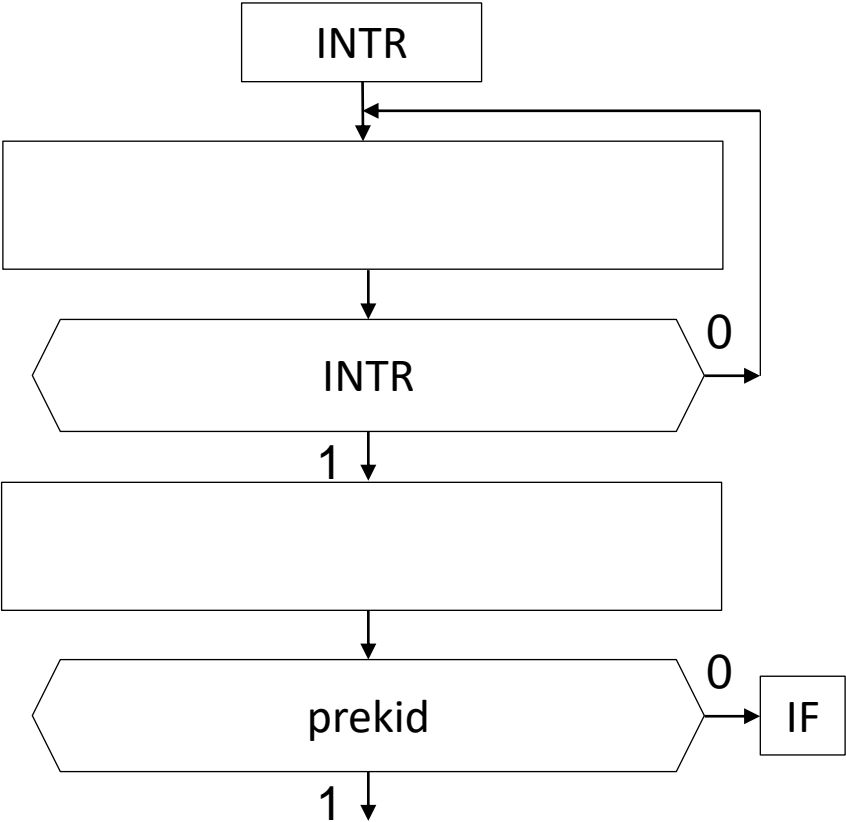




Управљачка јединица



step00 br(if notINTR then **step00**)
step01 br(if notprekid then **step**)



step00 br(if notINTR then **step00**)

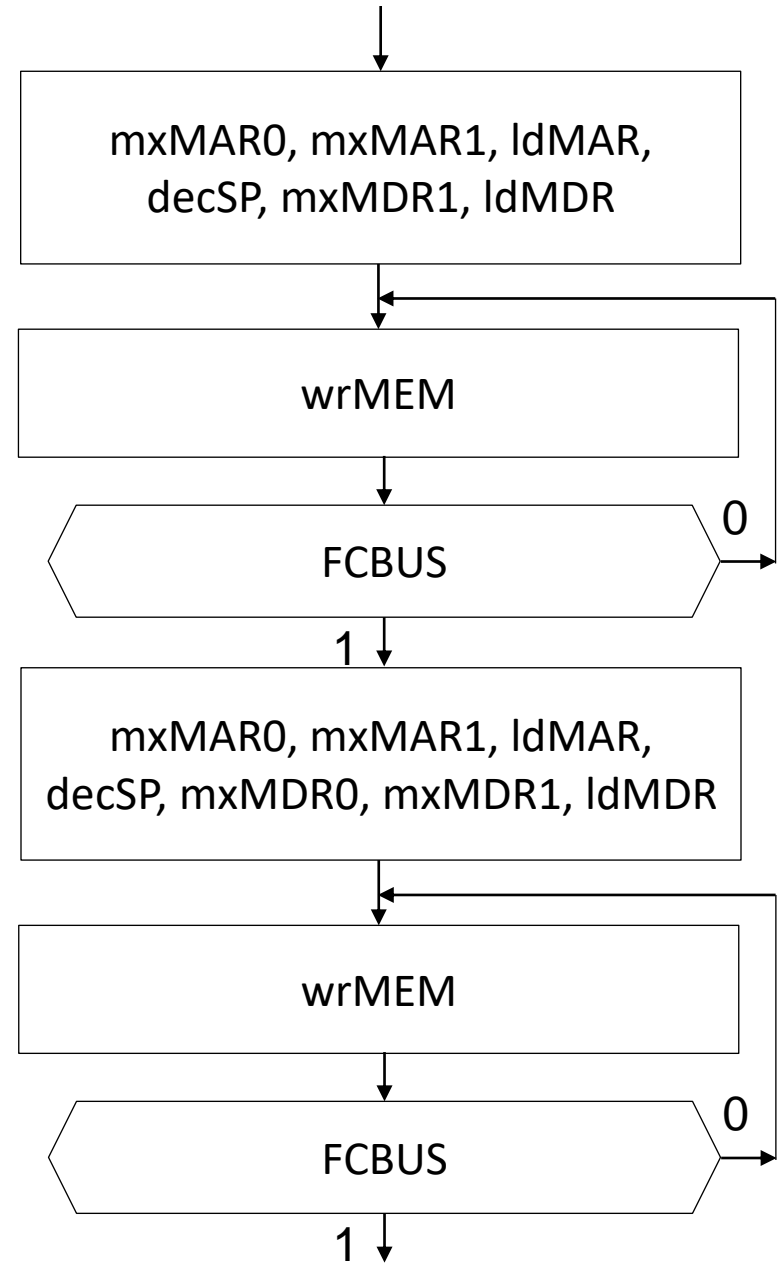
step01 br(if notprekid then **step**)

step02 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR

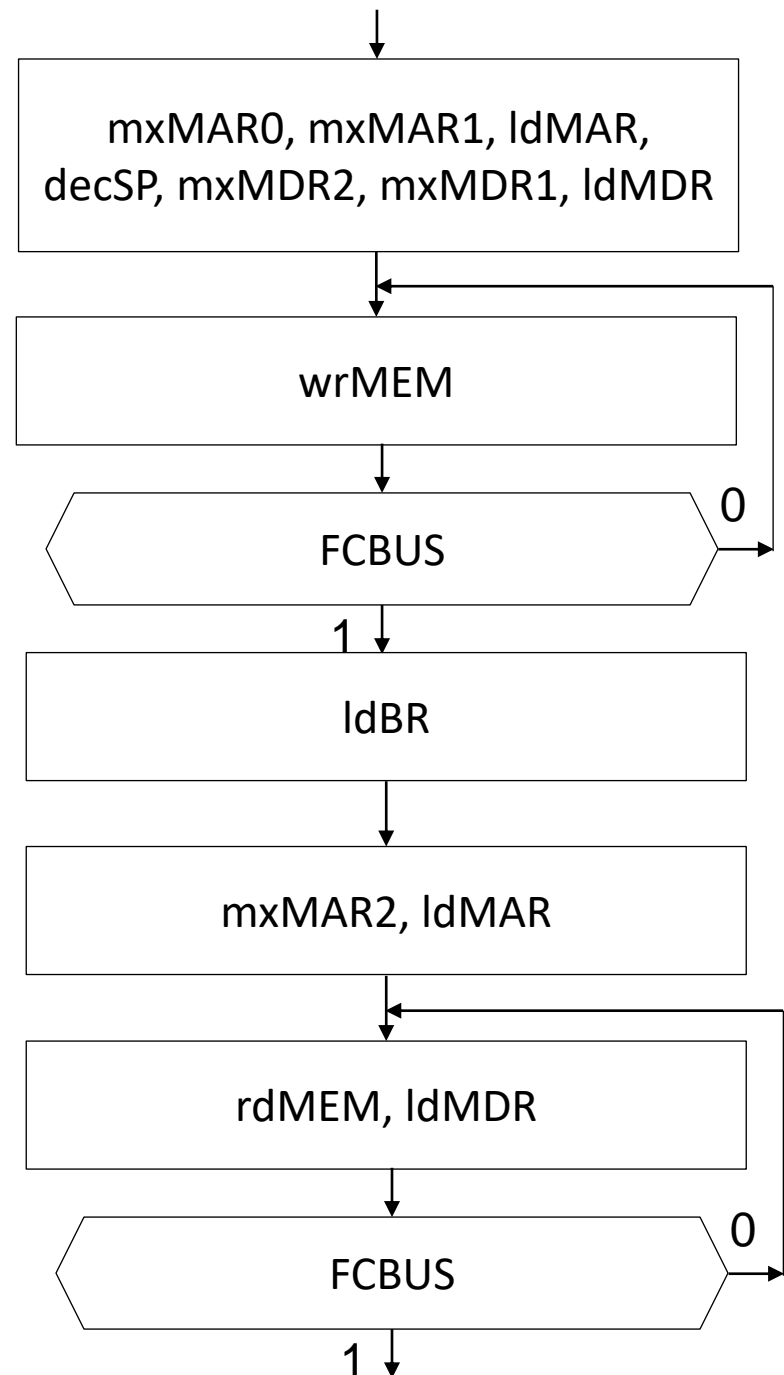
step03 wrMEM,
br(if notFCBUS then **step03**)

step04 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR0, mxMDR1, ldMDR

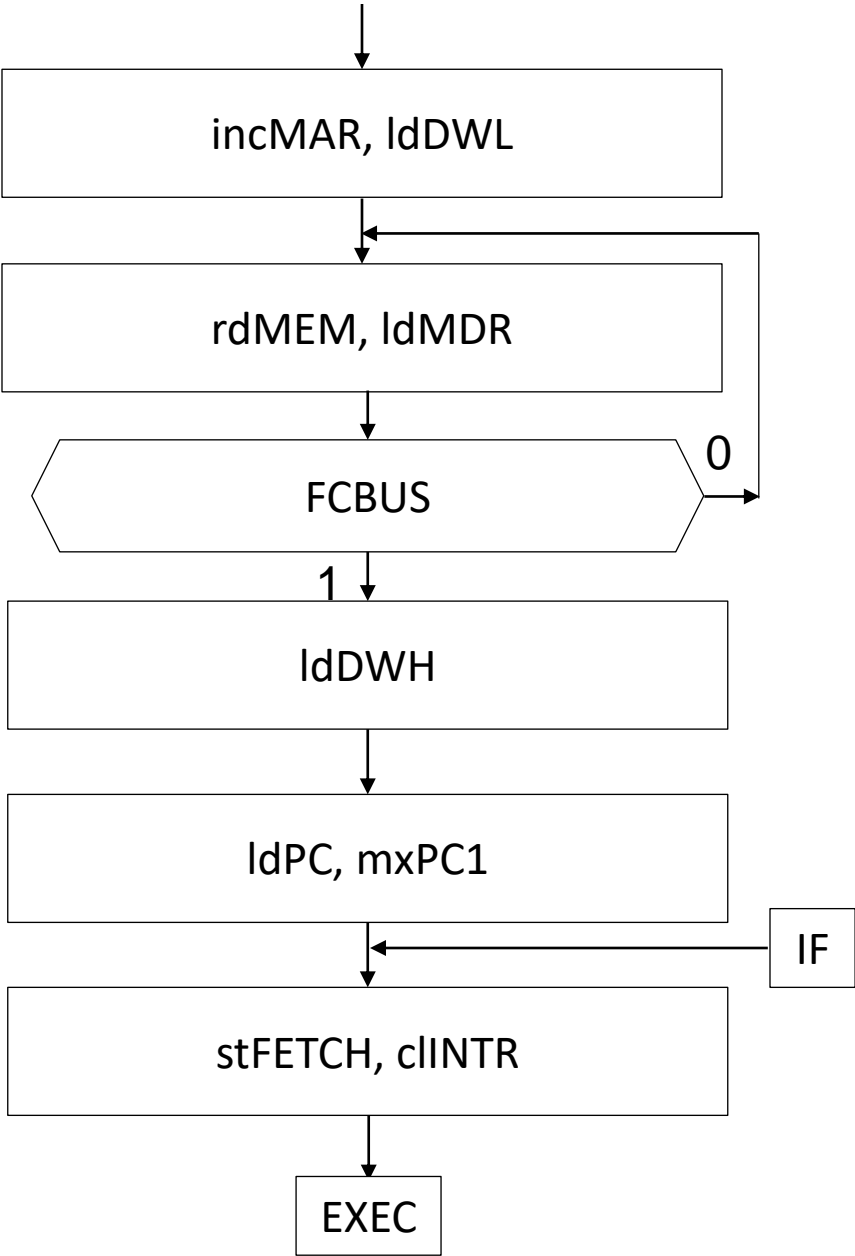
step05 wrMEM,
br(if notFCBUS then **step05**)



step00 br(if notINTR then **step00**)
step01 br(if notprekid then **step**)
step02 mxMAR0, mxMAR1, ldMAR,
 decSP, mxMDR1, ldMDR
step03 wrMEM,
 br(if notFCBUS then **step03**)
step04 mxMAR0, mxMAR1, ldMAR, decSP,
 mxMDR0, mxMDR1, ldMDR
step05 wrMEM,
 br(if notFCBUS then **step05**)
step06 mxMAR0,mxMAR1,ldMAR,decSP,
 mxMDR2,mxMDR1,ldMDR
step07 wrMEM,
 br(if notFCBUS then **step07**)
step08 ldBR
step09 mxMAR2, ldMAR
step0A rdMEM, ldMDR
 br(if notFCBUS then **step0A**)



step0B incMAR, ldDWL
step0C rdMEM, ldMDR
br(if notFCBUS then **step0C**)
step0D ldDWH
step0E ldPC, mxPC1
step0F stFETCH, cINTR,
br **step00**



step00 br(if notINTR then **step00**)
step01 br(if notprekid then **step**)
step02 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR
step03 wrMEM,
br(if notFCBUS then **step03**)
step04 mxMAR0, mxMAR1, ldMAR, decSP,
mxMDR0, mxMDR1, ldMDR
step05 wrMEM,
br(if notFCBUS then **step05**)
step06 mxMAR0,mxMAR1,ldMAR,decSP,
mxMDR2,mxMDR1,ldMDR
step07 wrMEM,
br(if notFCBUS then **step07**)
step08 ldBR
step09 mxMAR2, ldMAR
step0A rdMEM, ldMDR
br(if notFCBUS then **step0A**)

0	1	2	3
mxMAR0	mxMAR1	ldMAR	decSP

4	5	6	7
mxMDR1	ldMDR	wrMEM	mxMDR0

8	9	10	11
mxMDR2	ldBR	mxMAR2	rdMEM

12	13	14	15

16	17	18	19

20	21	22	23

step0B incMAR, ldDWL
step0C rdMEM, ldMDR
br(if notFCBUS then **step0C**)
step0D ldDWH
step0E ldPC, mxPC1
step0F stFETCH, clINTR
br **step00**

0	1	2	3
mxMAR0	mxMAR1	ldMAR	decSP

4	5	6	7
mxMDR1	ldMDR	wrMEM	mxMDR0

8	9	10	11
mxMDR2	ldBR	mxMAR2	rdMEM

12	13	14	15
incMAR	ldDWL	ldDWH	ldPC

16	17	18	19
mxPC1	stFETCH	clINTR	/

20	21	22	23

Сигнал безусловног скока	CC
bruncnd	1

Сигнал условног скока	CC	Сигнал услова
brnotINTR	2	$\overline{\text{INTR}}$
brnotprekid	3	$\overline{\text{prekid}}$
brnotFCBUS	4	$\overline{\text{FCBUS}}$

0	1	2	3	24	25	26	27
mxMAR0	mxMAR1	ldMAR	decSP	ba			
4	5	6	7	28	29	30	31
mxMDR1	ldMDR	wrMEM	mxMDR0	ba			
8	9	10	11				
mxMDR2	ldBR	mxMAR2	rdMEM				
12	13	14	15				
incMAR	ldDWL	ldDWH	ldPC				
16	17	18	19				
mxPC1	stFETCH	clINTR	/				
20	21	22	23				
cc							

step00 br(if notINTR then **step00**)

step01 br(if notprekid then **step0F**)

step02 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR

step03 wrMEM,
br(if notFCBUS then **step03**)

step04 mxMAR0, mxMAR1, ldMAR, decSP,
mxMDR0, mxMDR1, ldMDR

step05 wrMEM,
br(if notFCBUS then **step05**)

step06 mxMAR0, mxMAR1, ldMAR, decSP,
mxMDR2, mxMDR1, ldMDR

step07 wrMEM,
br(if notFCBUS then **step07**)

step08 ldBR

step09 mxMAR2, ldMAR

step0A rdMEM, ldMDR
br(if notFCBUS then **step0A**)

step0B incMAR, ldDWL

step0C rdMEM, ldMDR
br(if notFCBUS then **step0C**)

step0D ldDWH

step0E ldPC, mxPC1

step0F stFETCH, clINTR
br **step00**