

# **ОСНОВИ РАЧУНАРСКЕ ТЕХНИКЕ**

*FPGA*

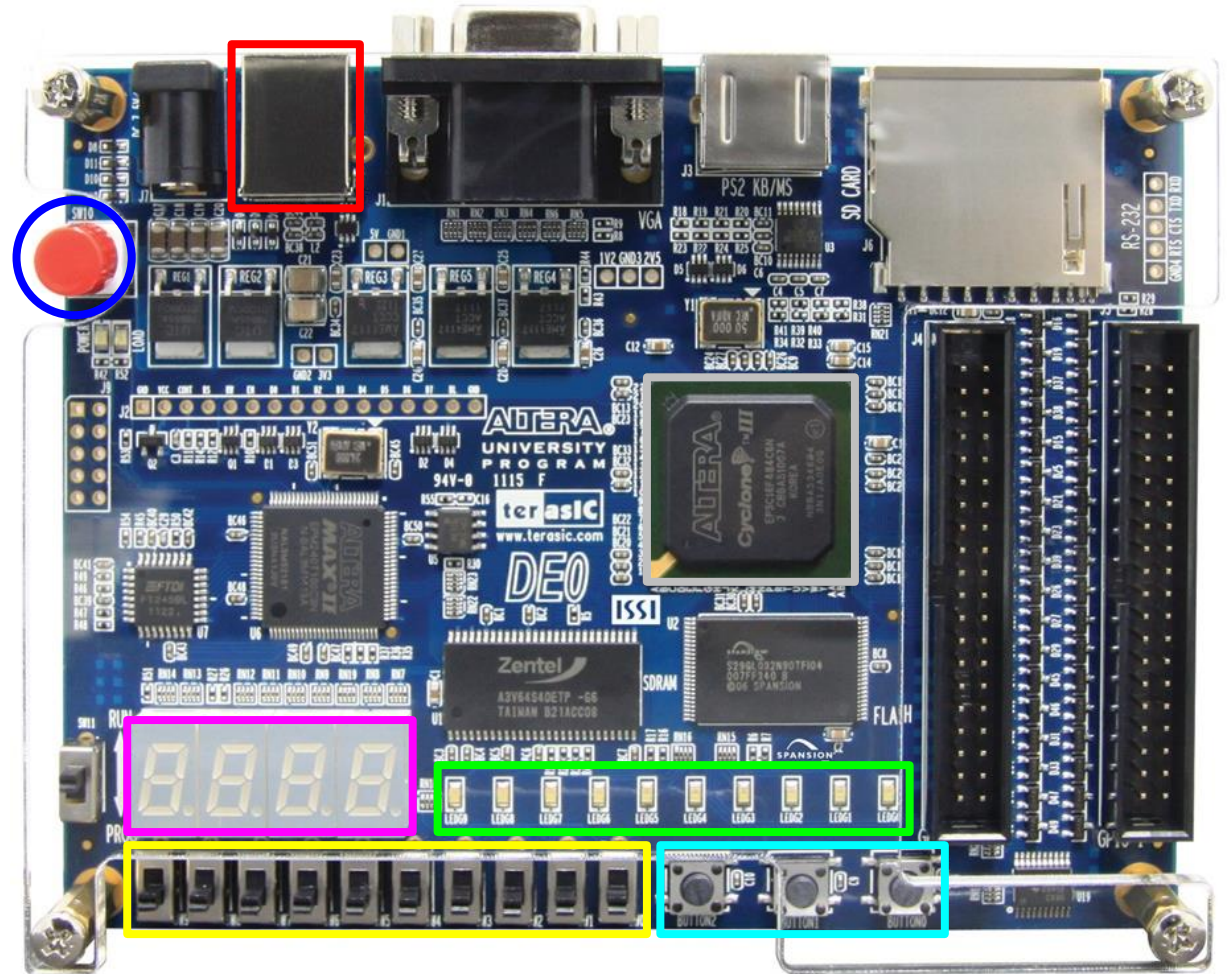
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# Плочица

- DE0

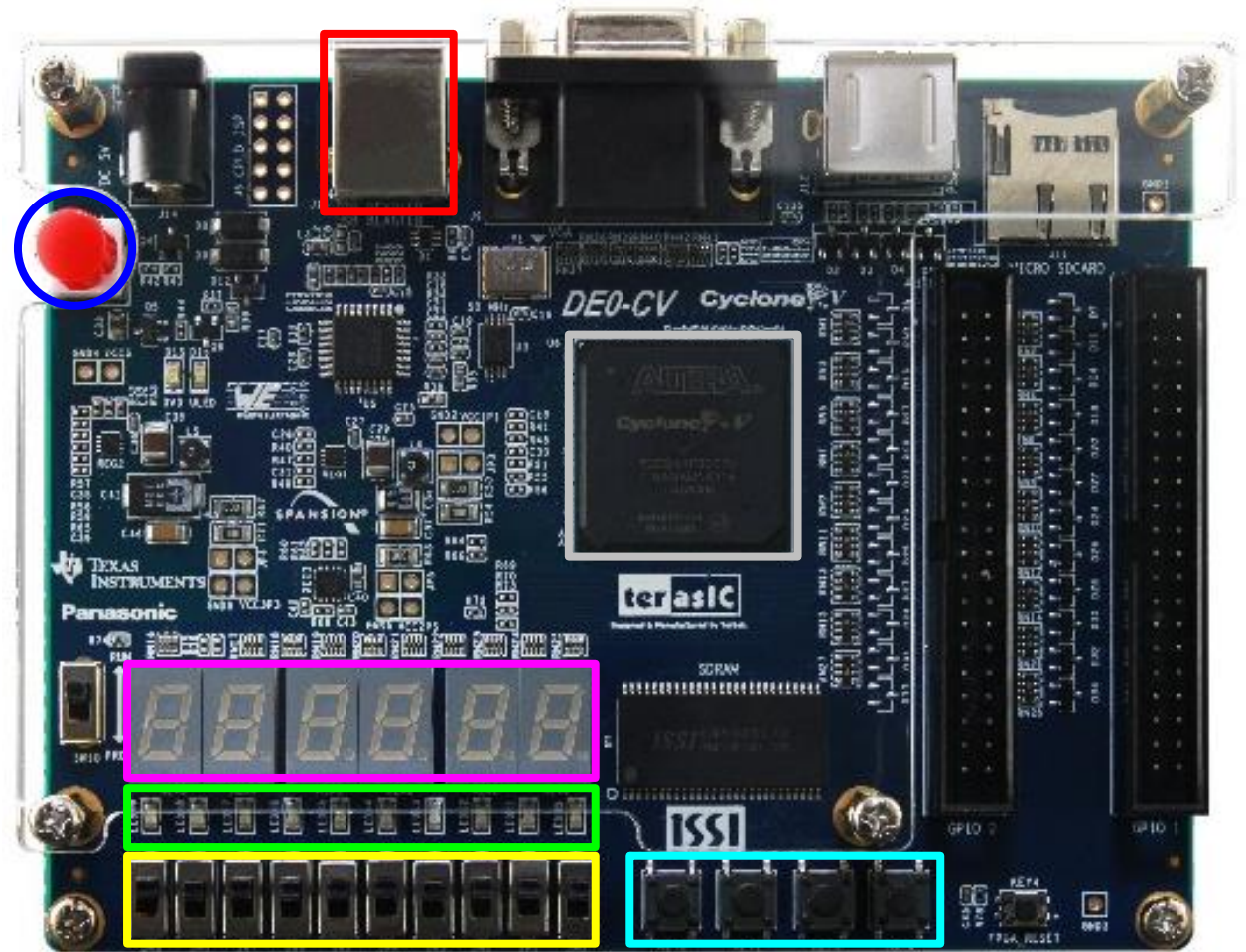
	Cyclone III EP3C16F484C6
	USB Blaster Connector
	Power ON/OFF Switch
	Switches
	Buttons
	LEDs
	7-Segment Displays



# Плочица

- DE0-CV

	Cyclone V 5CEBA4F23C7
	USB Blaster Connector
	Power ON/OFF Switch
	Switches
	Buttons
	LEDs
	7-Segment Displays



# ПИНОВИ

- Switches

Cyclone III		Cyclone V	
SW[0]	PIN_J6	SW0	PIN_U13
SW[1]	PIN_H5	SW1	PIN_V13
SW[2]	PIN_H6	SW2	PIN_T13
SW[3]	PIN_G4	SW3	PIN_T12
SW[4]	PIN_G5	SW4	PIN_AA15
SW[5]	PIN_J7	SW5	PIN_AB15
SW[6]	PIN_H7	SW6	PIN_AA14
SW[7]	PIN_E3	SW7	PIN_AA13
SW[8]	PIN_E4	SW8	PIN_AB13
SW[9]	PIN_D2	SW9	PIN_AB12

- Buttons

Cyclone III		Cyclone V	
BUTTON[0]	PIN_H2	KEY0	PIN_U7
BUTTON[1]	PIN_G3	KEY1	PIN_W9
BUTTON[2]	PIN_F1	KEY2	PIN_M7
-	-	KEY3	PIN_M6

- Clock

Cyclone III		Cyclone V	
CLOCK_50	PIN_G21	CLOCK_50	PIN_M9

# ПИНОВИ

- LEDs

Cyclone III		Cyclone V	
LEDG[0]	PIN_J1	LEDR0	PIN_AA2
LEDG[1]	PIN_J2	LEDR1	PIN_AA1
LEDG[2]	PIN_J3	LEDR2	PIN_W2
LEDG[3]	PIN_H1	LEDR3	PIN_Y3
LEDG[4]	PIN_F2	LEDR4	PIN_N2
LEDG[5]	PIN_E1	LEDR5	PIN_N1
LEDG[6]	PIN_C1	LEDR6	PIN_U2
LEDG[7]	PIN_C2	LEDR7	PIN_U1
LEDG[8]	PIN_B2	LEDR8	PIN_L2
LEDG[9]	PIN_B1	LEDR9	PIN_L1

- 7-Segment Displays

Cyclone III		Cyclone V	
HEX0_D[0]	PIN_E11	HEX00	PIN_U21
HEX0_D[1]	PIN_F11	HEX01	PIN_V21
HEX0_D[2]	PIN_H12	HEX02	PIN_W22
HEX0_D[3]	PIN_H13	HEX03	PIN_W21
HEX0_D[4]	PIN_G12	HEX04	PIN_Y22
HEX0_D[5]	PIN_F12	HEX05	PIN_Y21
HEX0_D[6]	PIN_F13	HEX06	PIN_AA22
HEX0_DP	PIN_D13	-	-
HEX1_D[0]	PIN_A13	HEX10	PIN_AA20
HEX1_D[1]	PIN_B13	HEX11	PIN_AB20

# ПИНОВИ

Cyclone III		Cyclone V	
HEX1_D[2]	PIN_C13	HEX12	PIN_AA19
HEX1_D[3]	PIN_A14	HEX13	PIN_AA18
HEX1_D[4]	PIN_B14	HEX14	PIN_AB18
HEX1_D[5]	PIN_E14	HEX15	PIN_AA17
HEX1_D[6]	PIN_A15	HEX16	PIN_U22
HEX1_DP	PIN_B15	-	-
HEX2_D[0]	PIN_D15	HEX20	PIN_Y19
HEX2_D[1]	PIN_A16	HEX21	PIN_AB17
HEX2_D[2]	PIN_B16	HEX22	PIN_AA10
HEX2_D[3]	PIN_E15	HEX23	PIN_Y14
HEX2_D[4]	PIN_A17	HEX24	PIN_V14

Cyclone III		Cyclone V	
HEX2_D[5]	PIN_B17	HEX25	PIN_AB22
HEX2_D[6]	PIN_F14	HEX26	PIN_AB21
HEX2_DP	PIN_A18	-	-
HEX3_D[0]	PIN_B18	HEX30	PIN_Y16
HEX3_D[1]	PIN_F15	HEX31	PIN_W16
HEX3_D[2]	PIN_A19	HEX32	PIN_Y17
HEX3_D[3]	PIN_B19	HEX33	PIN_V16
HEX3_D[4]	PIN_C19	HEX34	PIN_U17
HEX3_D[5]	PIN_D19	HEX35	PIN_V18
HEX3_D[6]	PIN_G15	HEX36	PIN_V19
HEX3_DP	PIN_G16	-	-

# Преузимање алата

- <https://www.intel.com/content/www/us/en/software-kit/666221/intel-quartus-ii-web-edition-design-software-version-13-1-for-windows.html>
- Downloads -> Individual Files -> Intel Quartus Software -> ModelSim-Intel Edition
- Downloads -> Individual Files -> Intel Quartus Software -> Intel Quartus II Software
- Downloads -> Individual Files -> Devices -> Intel Cyclone III, Intel Cyclone IV Device Support
- Downloads -> Individual Files -> Devices -> Intel Cyclone V Device Support





Project Navigator

Compilation Hierarchy

Hierarchy | Files | Design Units

Tasks

Flow: Compilation

Task	
▶	Compile Design
▶▶	Analysis & Synthesis
▶▶	Fitter (Place & Route)
▶▶	Assembler (Generate programming files)
▶▶	TimeQuest Timing Analysis
▶▶	EDA Netlist Writer
▶	Program Device (Open Programmer)



- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

Messages

All [Error] [Warning] [Info] [Search]

Type	ID	Message

System | Processing

# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
- Family & Device Settings [page 3 o f 5] -> Device family -> Name filter -> Available devices -> Next
- EDA Tool Settings [page 4 o f 5] -> Next
- Summary [page 5 o f 5] -> Finish



- New... Ctrl+N
- Open... Ctrl+O
- Close Ctrl+F4
- New Project Wizard...**
- Open Project... Ctrl+J
- Save Project
- Close Project
- Save Ctrl+S
- Save As...
- Save All Ctrl+Shift+S
- File Properties...
- Create / Update
- Export...
- Convert Programming Files...
- Page Setup...
- Print Preview
- Print... Ctrl+P
- Recent Files
- Recent Projects
- Exit Alt+F4

# ALTERA

# QUARTUS® II

Version 13.1

Flow: Compilation Customize...

Task	
▼	▶ Compile Design
>	▶ Analysis & Synthesis
>	▶ Fitter (Place & Route)
>	▶ Assembler (Generate programming files)
>	▶ TimeQuest Timing Analysis
>	▶ EDA Netlist Writer
🖱	Program Device (Open Programmer)

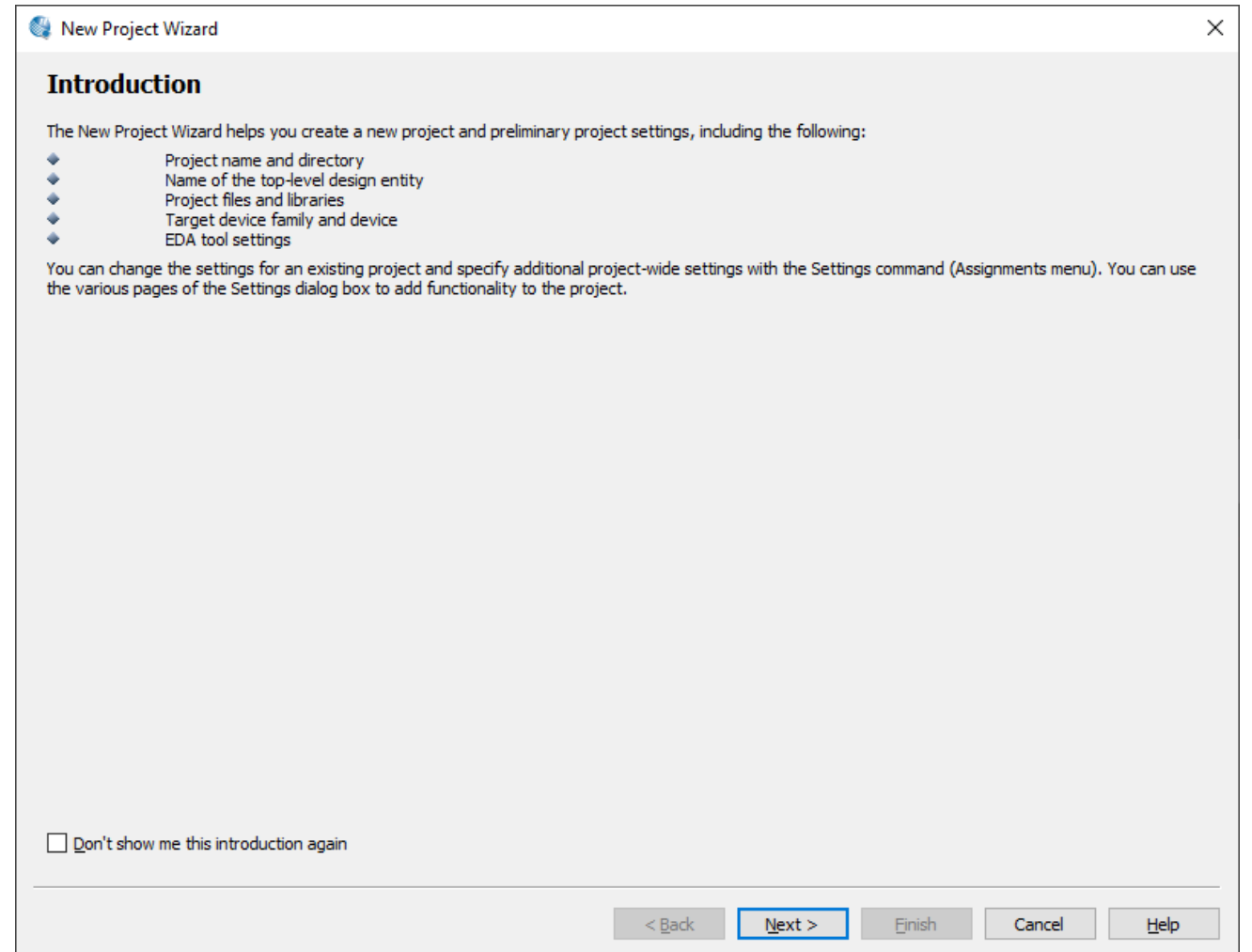
- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

All [Icons] <<Search>>

Type	ID	Message

# Прављење пројекта

- File -> New Project Wizard...
- **Introduction -> Next**
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
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- Summary [page 5 o f 5] -> Finish



# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- **Directory, Name, Top-Level Entity [page 1 of 5] -> Directory -> Name -> Top-Level Entity -> Next**
- Add Files [page 2 of 5] -> Next
- Family & Device Settings [page 3 of 5] -> Device family -> Name filter -> Available devices -> Next
- EDA Tool Settings [page 4 of 5] -> Next
- Summary [page 5 of 5] -> Finish

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:/Users/aleksas/Desktop/Direktorijum ...

What is the name of this project?

Naziv ...

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

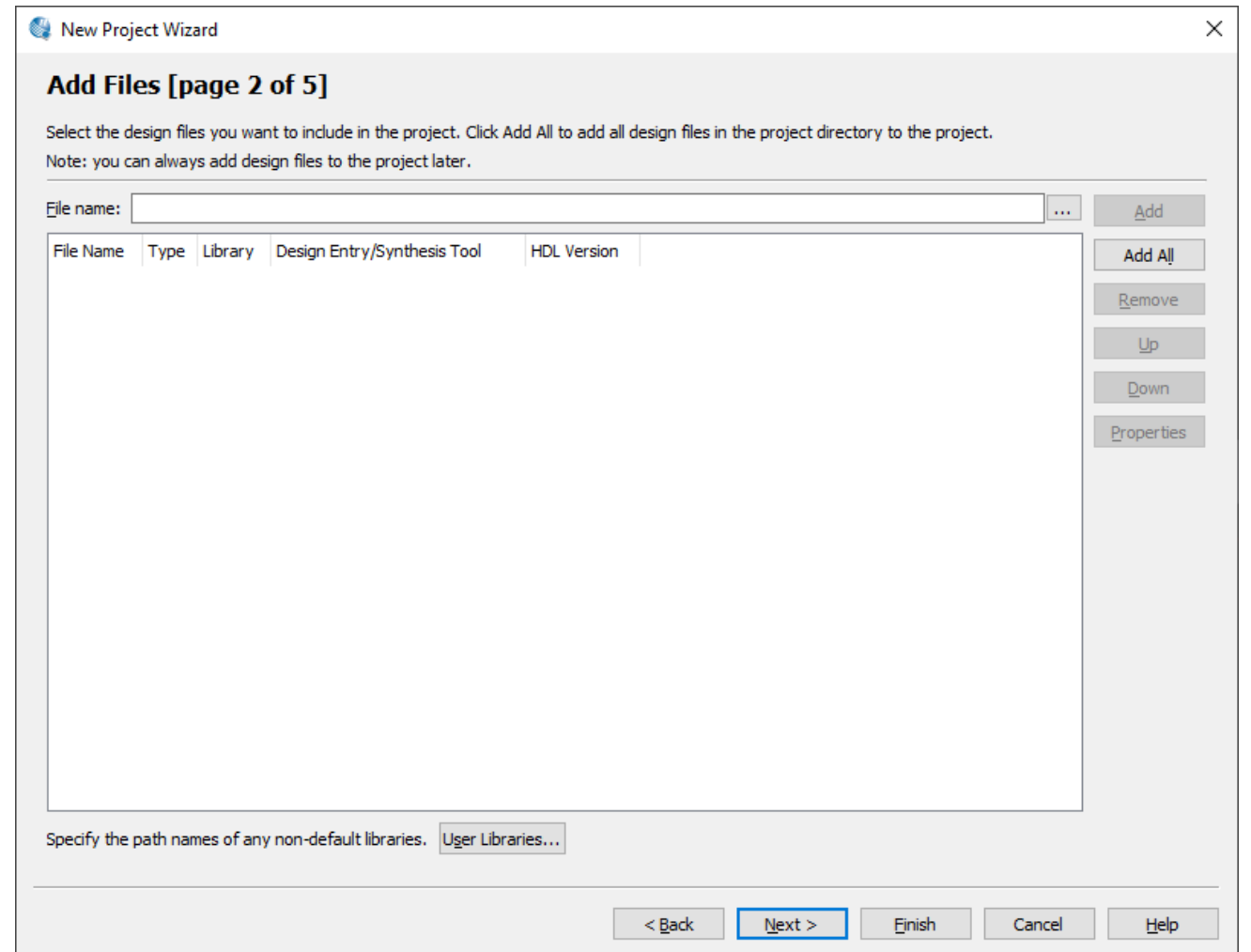
Glavna ...

Use Existing Project Settings...

< Back Next > Finish Cancel Help

# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- **Add Files [page 2 o f 5] -> Next**
- Family & Device Settings [page 3 o f 5] -> Device family -> Name filter -> Available devices -> Next
- EDA Tool Settings [page 4 o f 5] -> Next
- Summary [page 5 o f 5] -> Finish



# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
- **Family & Device Settings [page 3 o f 5]**  
-> Device family: Cyclone III -> Name filter: EP3C16F484C6 -> Available devices -> Next
- EDA Tool Settings [page 4 o f 5] -> Next
- Summary [page 5 o f 5] -> Finish

The screenshot shows the 'New Project Wizard' dialog box, page 3 of 5, titled 'Family & Device Settings'. The window contains the following elements:

- Device family:** Family: Cyclone III, Devices: All
- Target device:** Radio buttons for 'Auto device selected by the Fitter', 'Specific device selected in 'Available devices' list' (selected), and 'Other: n/a'.
- Show in 'Available devices' list:** Package: Any, Pin count: Any, Speed grade: Any, Name filter: EP3C16F484C6, and a checked checkbox for 'Show advanced devices'.
- Available devices:** A table with the following data:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	bal Clo
EP3C16F484C6	1.2V	15408	347	516096	112	4	20

At the bottom of the dialog, there are navigation buttons: '< Back', 'Next >' (highlighted), 'Finish', 'Cancel', and 'Help'.

# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
- **Family & Device Settings [page 3 o f 5]**  
-> Device family: Cyclone V -> Name filter: 5CEBA4F23C7 -> Available devices -> Next
- EDA Tool Settings [page 4 o f 5] -> Next
- Summary [page 5 o f 5] -> Finish

The screenshot shows the 'New Project Wizard' dialog box, specifically the 'Family & Device Settings' page (page 3 of 5). The dialog is titled 'New Project Wizard' and has a close button in the top right corner. The main heading is 'Family & Device Settings [page 3 of 5]'. Below the heading, there is a sub-heading 'Family & Device Settings [page 3 of 5]' and a brief instruction: 'Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.'

The dialog is divided into several sections:

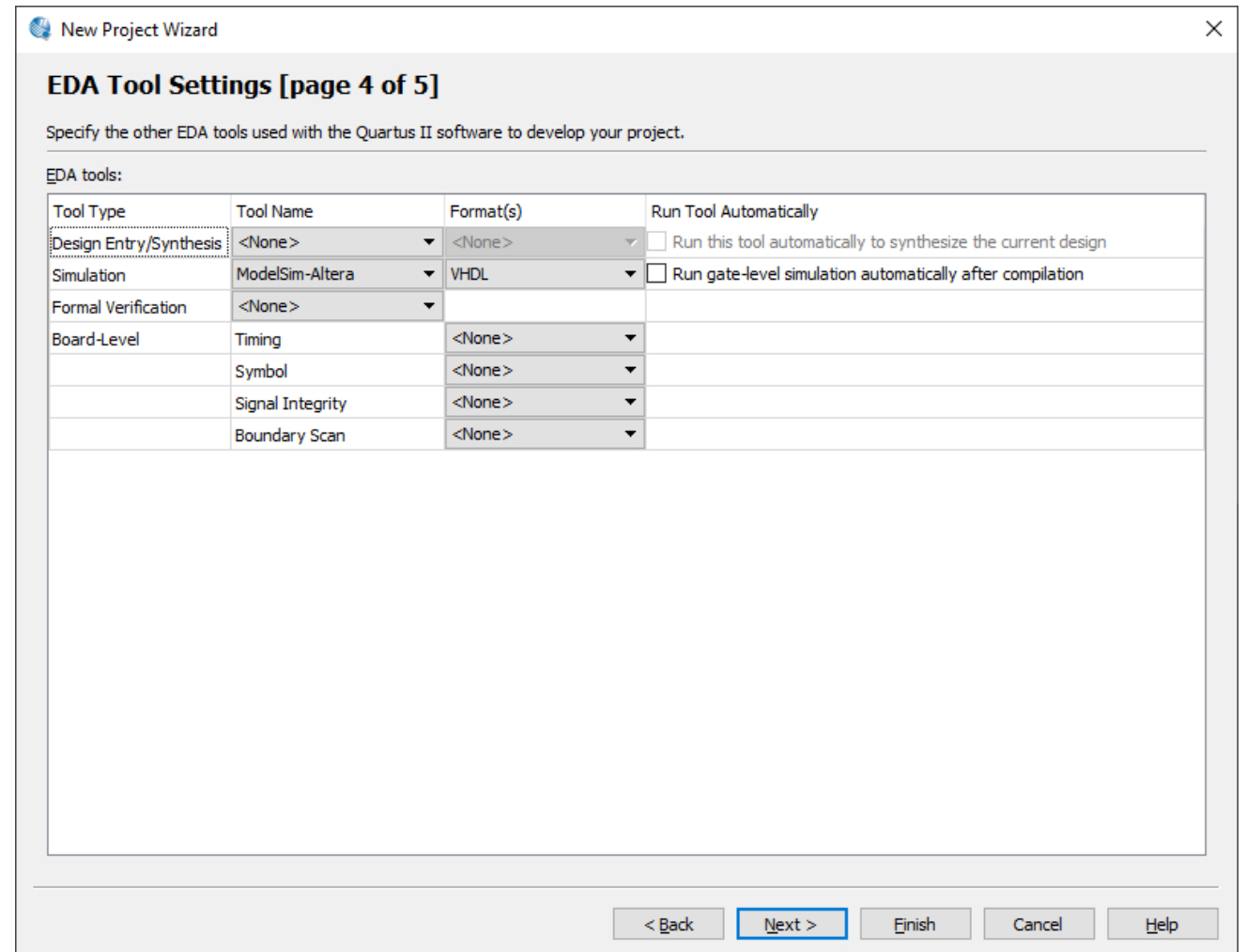
- Device family:** A dropdown menu for 'Family' is set to 'Cyclone V (E/GX/GT/SX/SE/ST)'. A 'Devices' dropdown is set to 'All'.
- Target device:** Three radio buttons are present: 'Auto device selected by the Fitter' (unselected), 'Specific device selected in 'Available devices' list' (selected), and 'Other: n/a' (unselected).
- Show in 'Available devices' list:** A group of settings including:
  - 'Package:' dropdown set to 'Any'
  - 'Pin count:' dropdown set to 'Any'
  - 'Speed grade:' dropdown set to 'Any'
  - 'Name filter:' text box containing '5CEBA4F23C7'
  - 'Show advanced devices' checkbox, which is checked.
- Available devices:** A table listing available devices. The table has columns for Name, Core Voltage, ALMs, User I/Os, GXB Channel PMA, GXB Channel PCS, and PCIe (PIPE) Hard IP Blocks. One device is listed: '5CEBA4F23C7' with a core voltage of 1.1V, 18480 ALMs, 224 User I/Os, 0 GXB Channel PMA, 0 GXB Channel PCS, and 0 PCIe (PIPE) Hard IP Blocks.

At the bottom of the dialog, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.



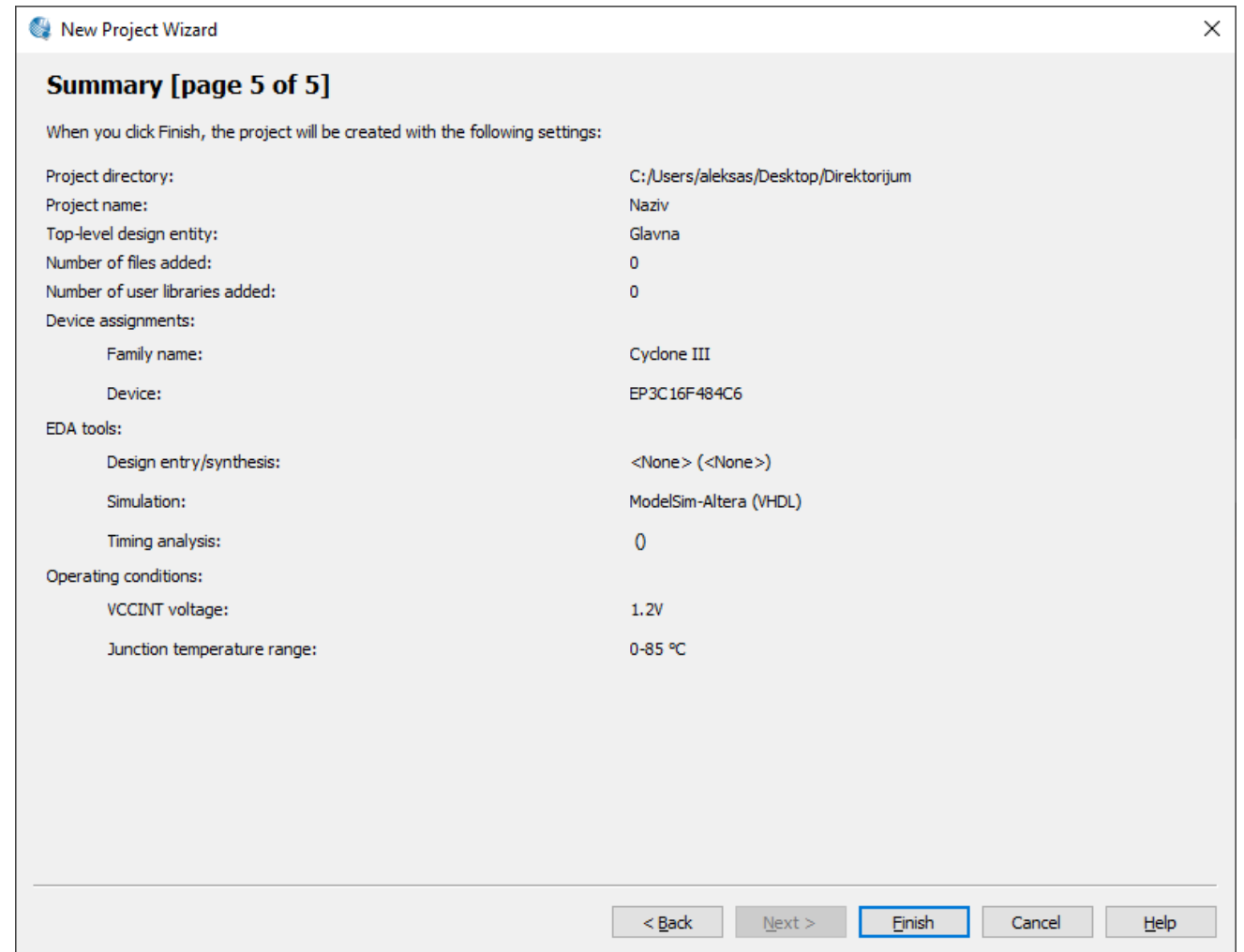
# Прављење пројекта

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- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
- Family & Device Settings [page 3 o f 5] -> Device family -> Name filter -> Available devices -> Next
- **EDA Tool Settings [page 4 o f 5] -> Next**
- Summary [page 5 o f 5] -> Finish



# Прављење пројекта

- File -> New Project Wizard...
- Introduction -> Next
- Directory, Name, Top-Level Entity [page 1 o f 5] -> Directory -> Name -> Top-Level Entity -> Next
- Add Files [page 2 o f 5] -> Next
- Family & Device Settings [page 3 o f 5] -> Device family -> Name filter -> Available devices -> Next
- EDA Tool Settings [page 4 o f 5] -> Next
- **Summary [page 5 o f 5] -> Finish**



Project Navigator

Entity

⚠ Cystone III: EP3C16F484C6

➤ Glavna

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
▼ Compile Design
> Analysis & Synthesis
> Fitter (Place & Route)
> Assembler (Generate programming files)
> TimeQuest Timing Analysis
> EDA Netlist Writer
🖱 Program Device (Open Programmer)



- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

Messages

All [Error] [Warning] [Info] [Help] <<Search>>

Type	ID	Message
System / Processing		

Project Navigator

Files

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
▶ Compile Design
▶ Analysis & Synthesis
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▶ Program Device (Open Programmer)

ALTERA

QUARTUS® II

Version 13.1

- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

Messages

All <<Search>>

Type	ID	Message
System		Processing

# Додавање шеме у пројекат

- File -> New...
- Design Files -> Block Diagram/Schematic File -> OK
- File -> Save As...
- File Name -> Add file to current project -> Save



- New... Ctrl+N
- Open... Ctrl+O
- Close Ctrl+F4
- New Project Wizard...
- Open Project... Ctrl+J
- Save Project
- Close Project
- Save Ctrl+S
- Save As...
- Save All Ctrl+Shift+S
- File Properties...
- Create / Update
- Export...
- Convert Programming Files...
- Page Setup...
- Print Preview
- Print... Ctrl+P
- Recent Files
- Recent Projects
- Exit Alt+F4

# ALTERA

# QUARTUS<sup>®</sup> II

Version 13.1

Flow: Compilation Customize...

- Task
- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Programmer)

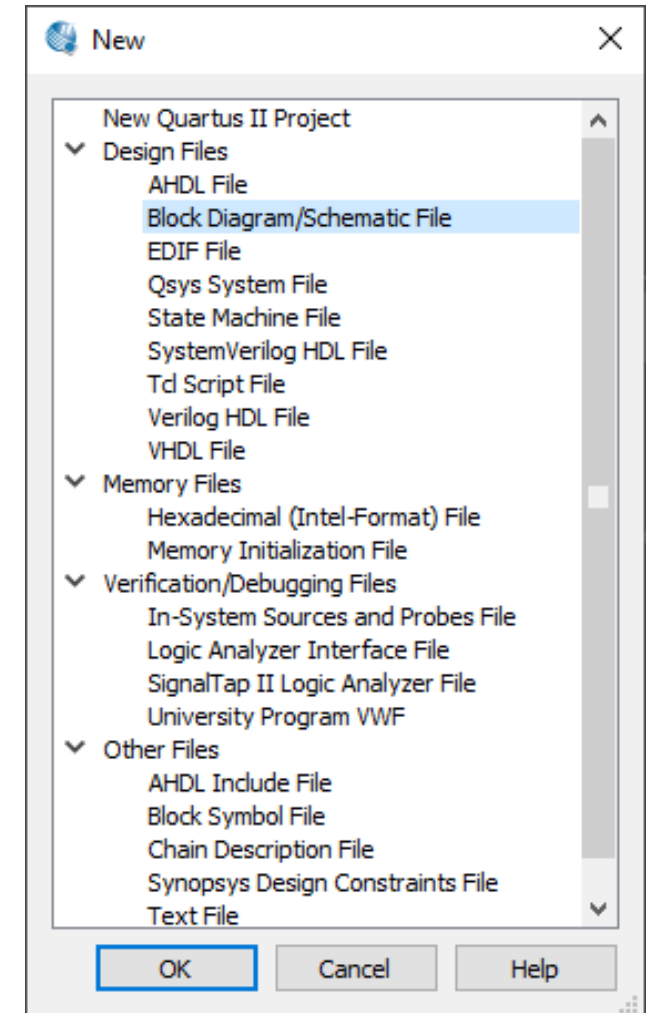
- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

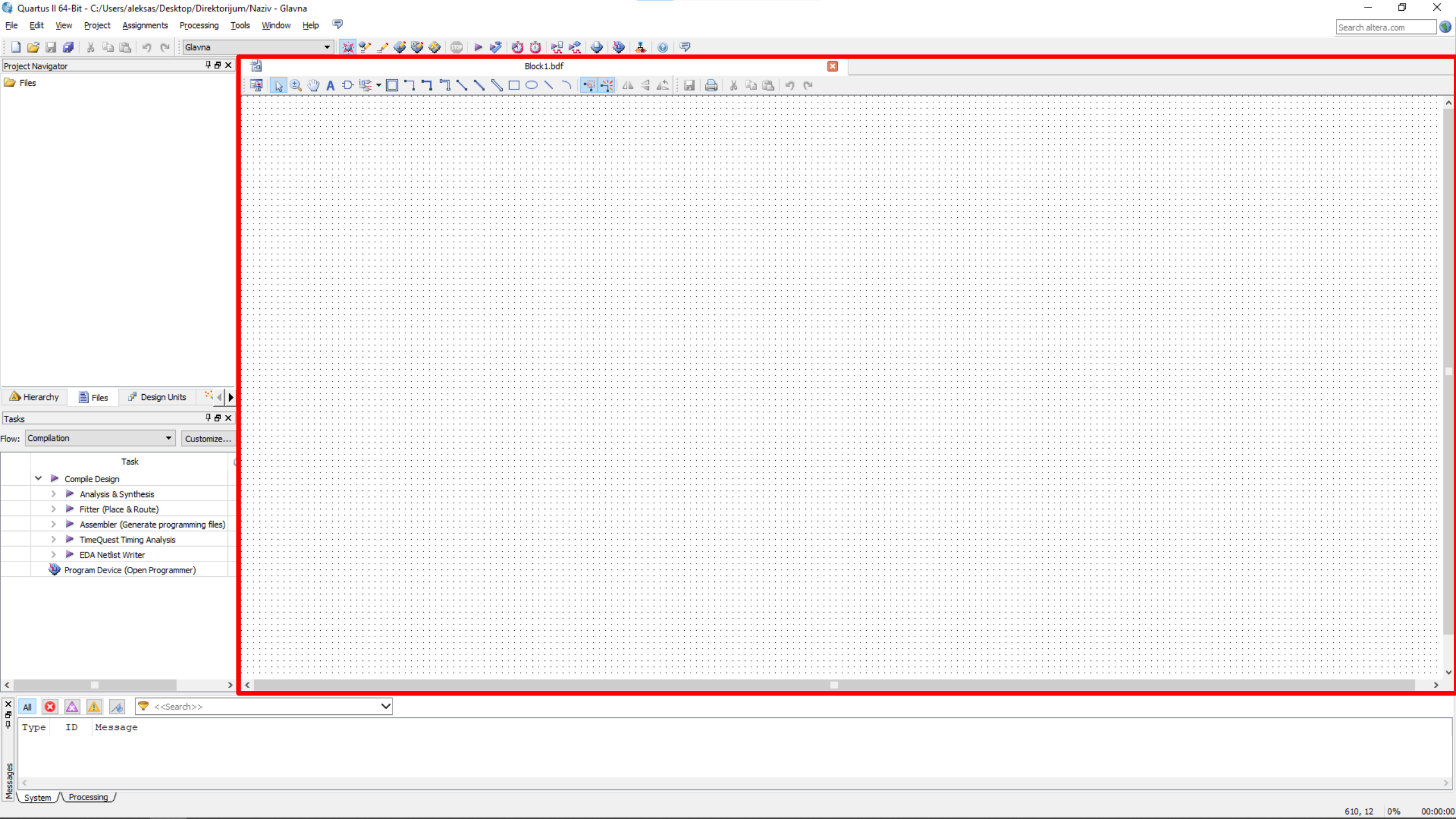
All <<Search>>

Type	ID	Message
System		Creates a new file

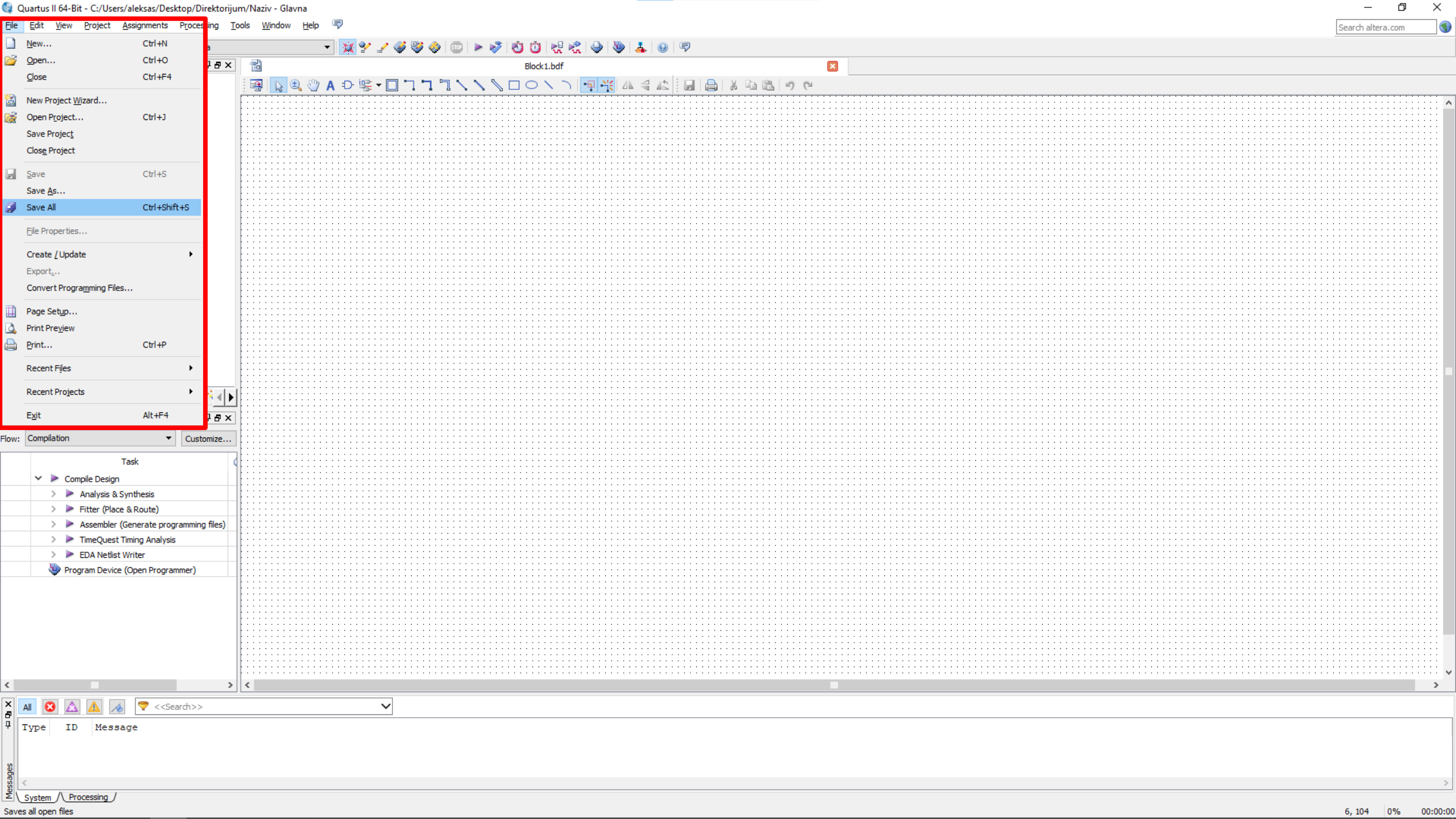
# Додавање шеме у пројекат

- File -> New...
- **Design Files -> Block Diagram/Schematic File -> OK**
- File -> Save As...
- File Name -> Add file to current project -> Save









- File
  - Edit
  - View
  - Project
  - Assignments
  - Processing
  - Tools
  - Window
  - Help
- New... Ctrl+N
  - Open... Ctrl+O
  - Close Ctrl+F4
  - New Project Wizard...
  - Open Project... Ctrl+J
  - Save Project
  - Close Project
  - Save Ctrl+S
  - Save As...
  - Save All Ctrl+Shift+S**
  - File Properties...
  - Create / Update
  - Export...
  - Convert Programming Files...
  - Page Setup...
  - Print Preview
  - Print... Ctrl+P
  - Recent Files
  - Recent Projects
  - Exit Alt+F4

Block1.bdf

Toolbar icons: Selection tools, Drawing tools, Navigation tools, Undo/Redo, Copy/Paste, Print, etc.

Main workspace: A large grid area for drawing logic diagrams.

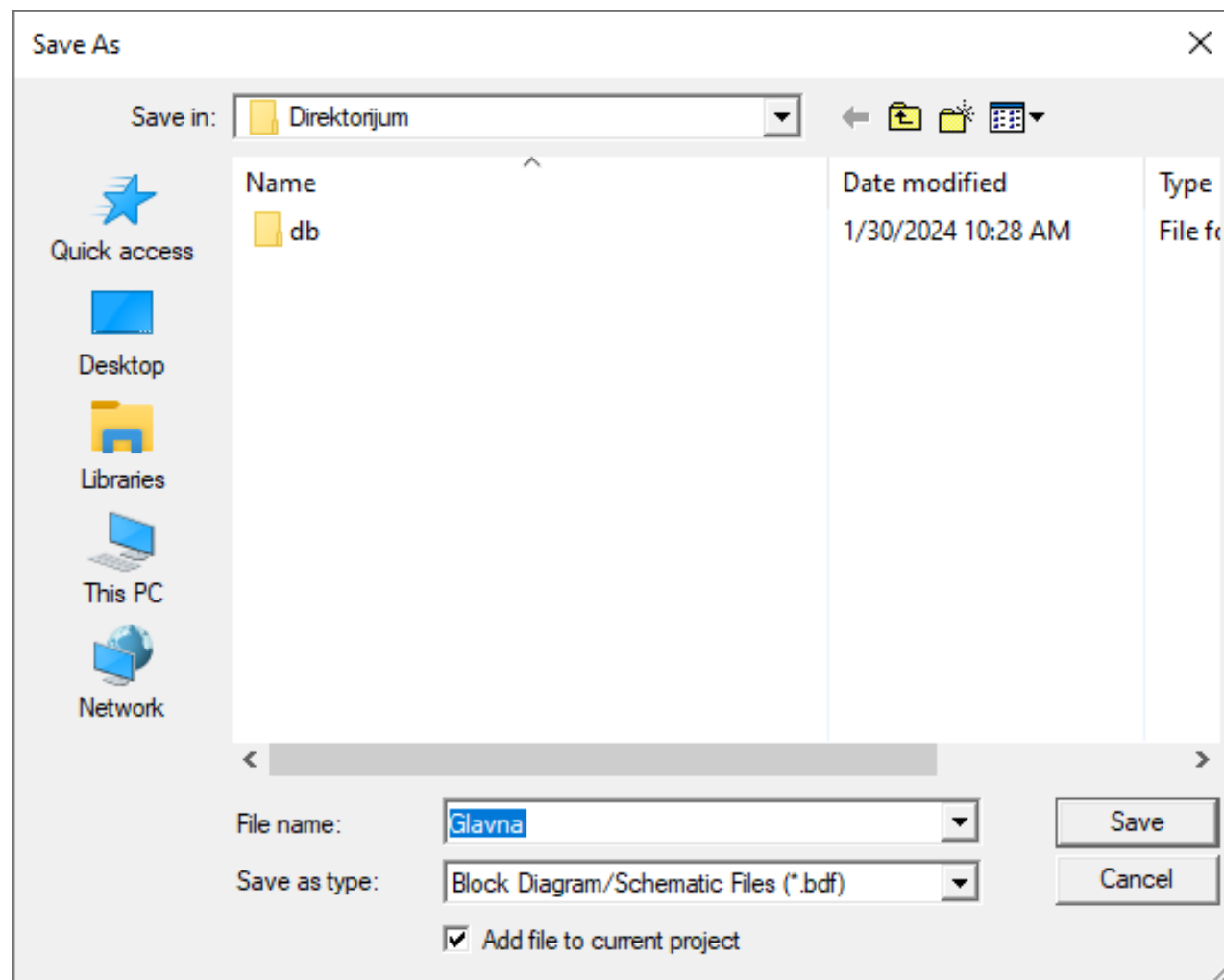
- Flow: Compilation Customize...
- Task
- Compile Design
    - Analysis & Synthesis
    - Fitter (Place & Route)
    - Assembler (Generate programming files)
    - TimeQuest Timing Analysis
    - EDA Netlist Writer
    - Program Device (Open Programmer)

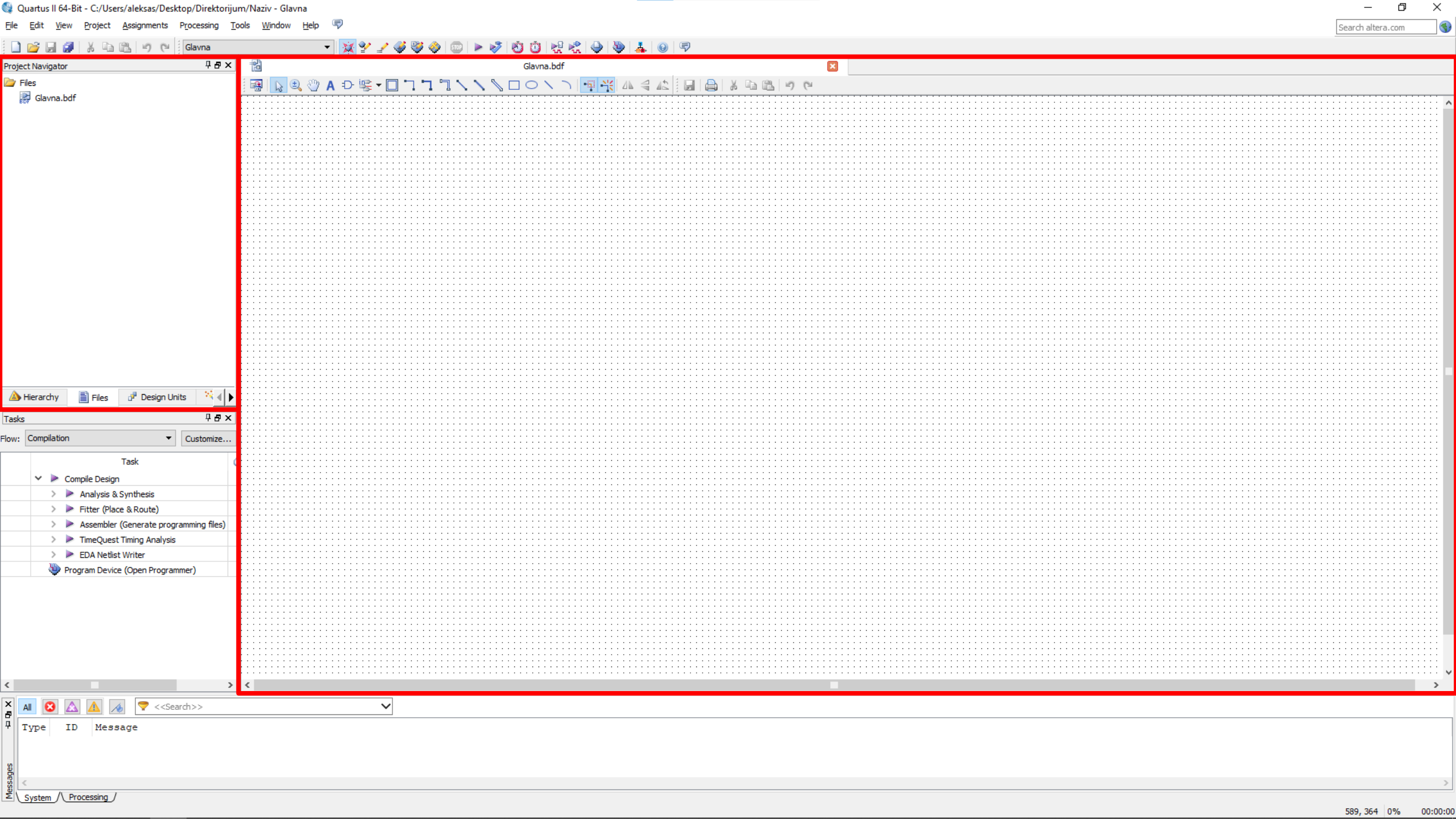
All [Icons] <<Search>>

Type	ID	Message

# Додавање шеме у пројекат

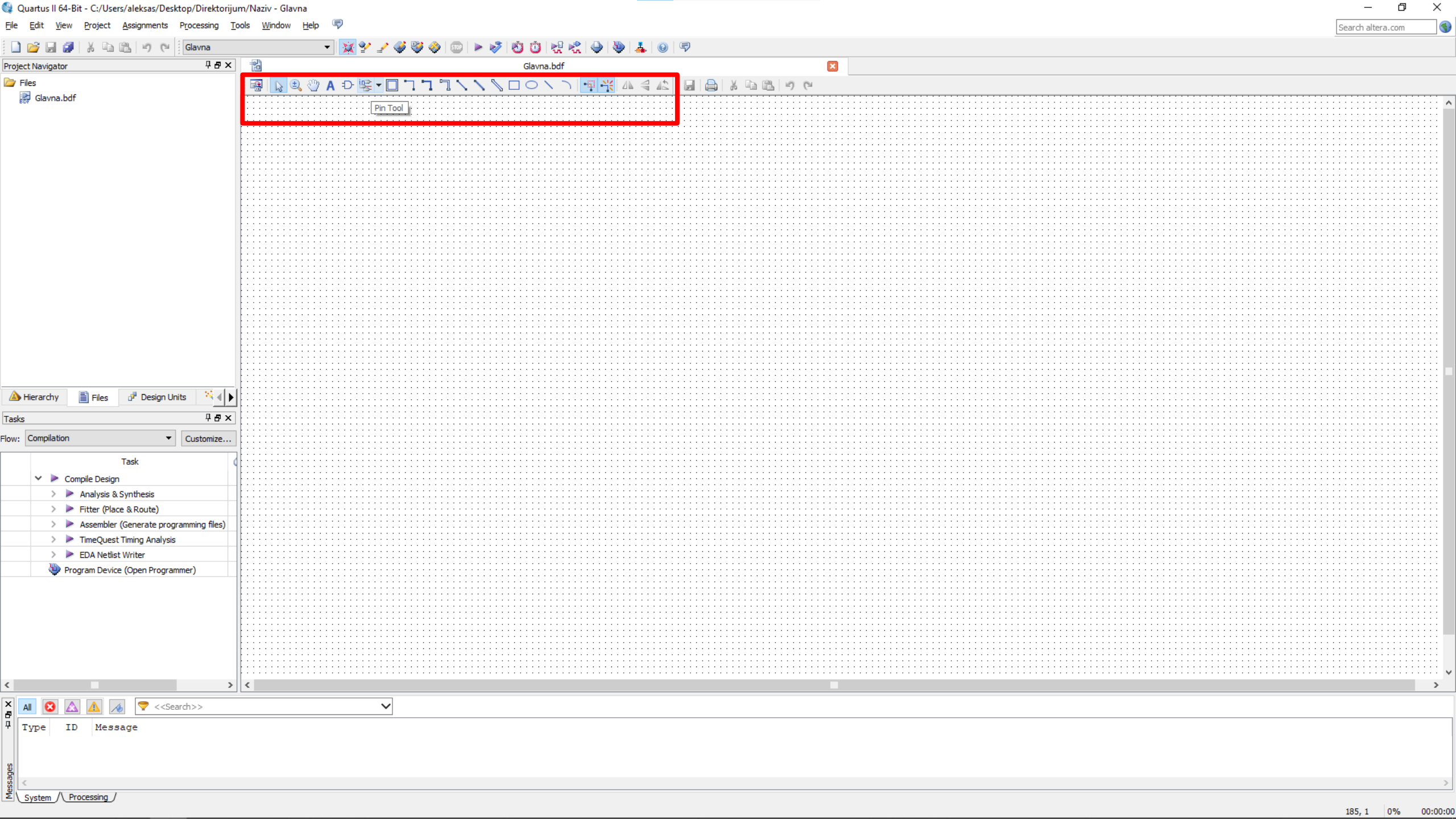
- File -> New...
- Design Files -> Block Diagram/Schematic File -> OK
- File -> Save As...
- **File Name -> Add file to current project -> Save**

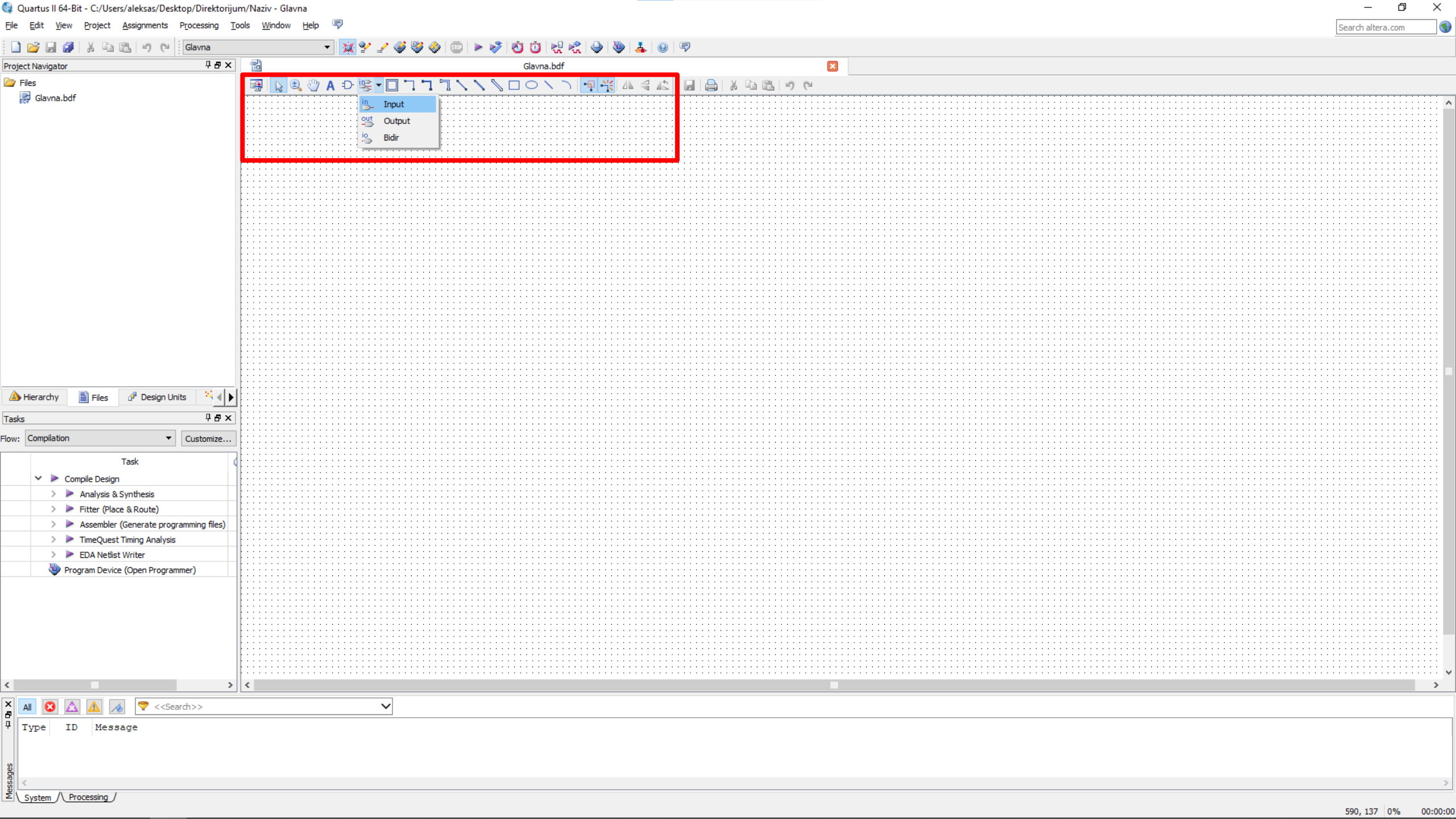


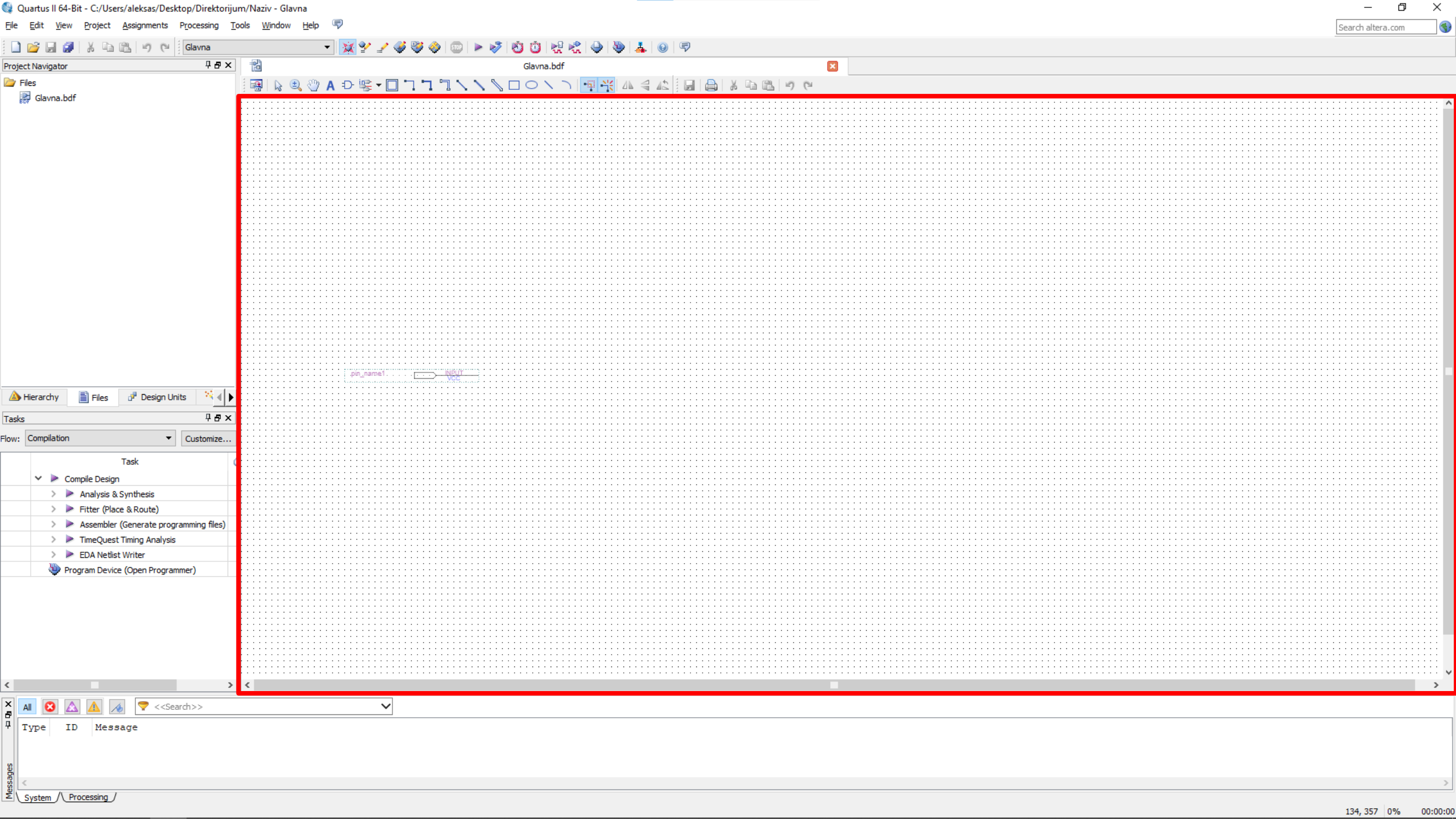


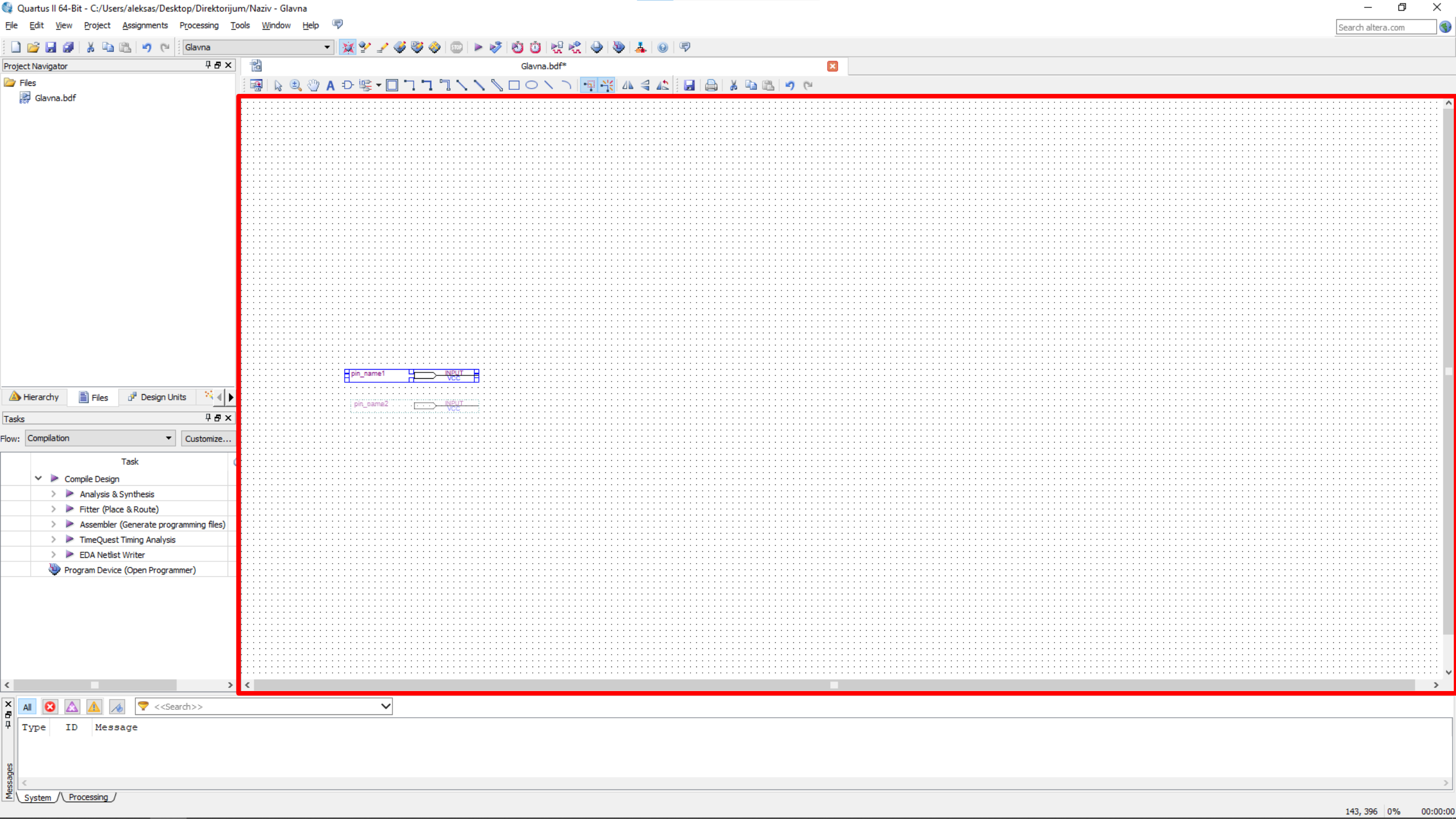
## Цртање шеме

- Block Editor -> Pin Tool -> Input -> Left Click -> Esc
- View -> Zoom In (Ctrl+Scroll)
- Block Editor -> Pin Tool -> Output -> Left Click -> Esc
- Block Editor -> Orthogonal Node Tool -> Left Click & Drag -> Esc
- File -> Save (Ctrl+S)

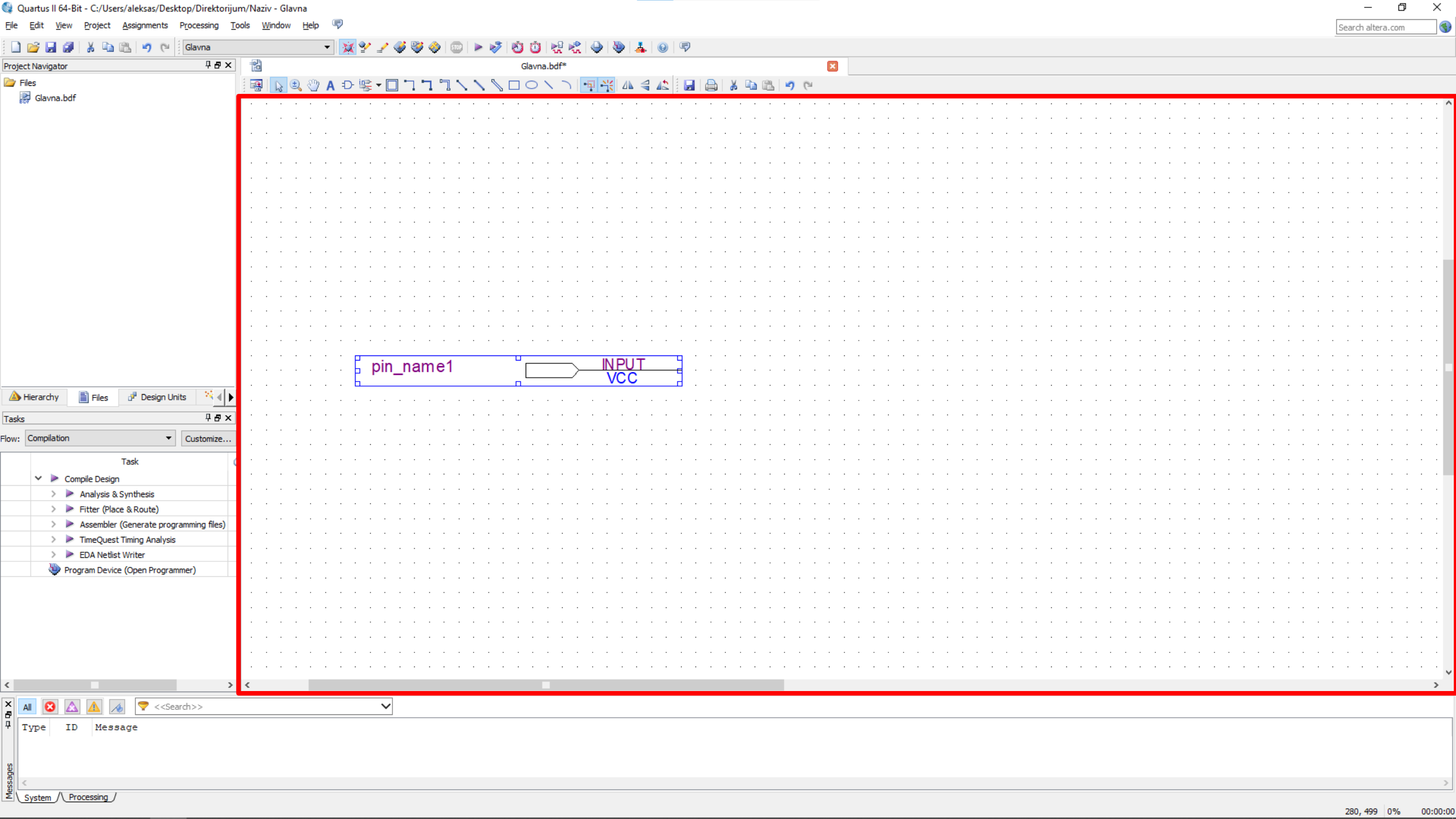








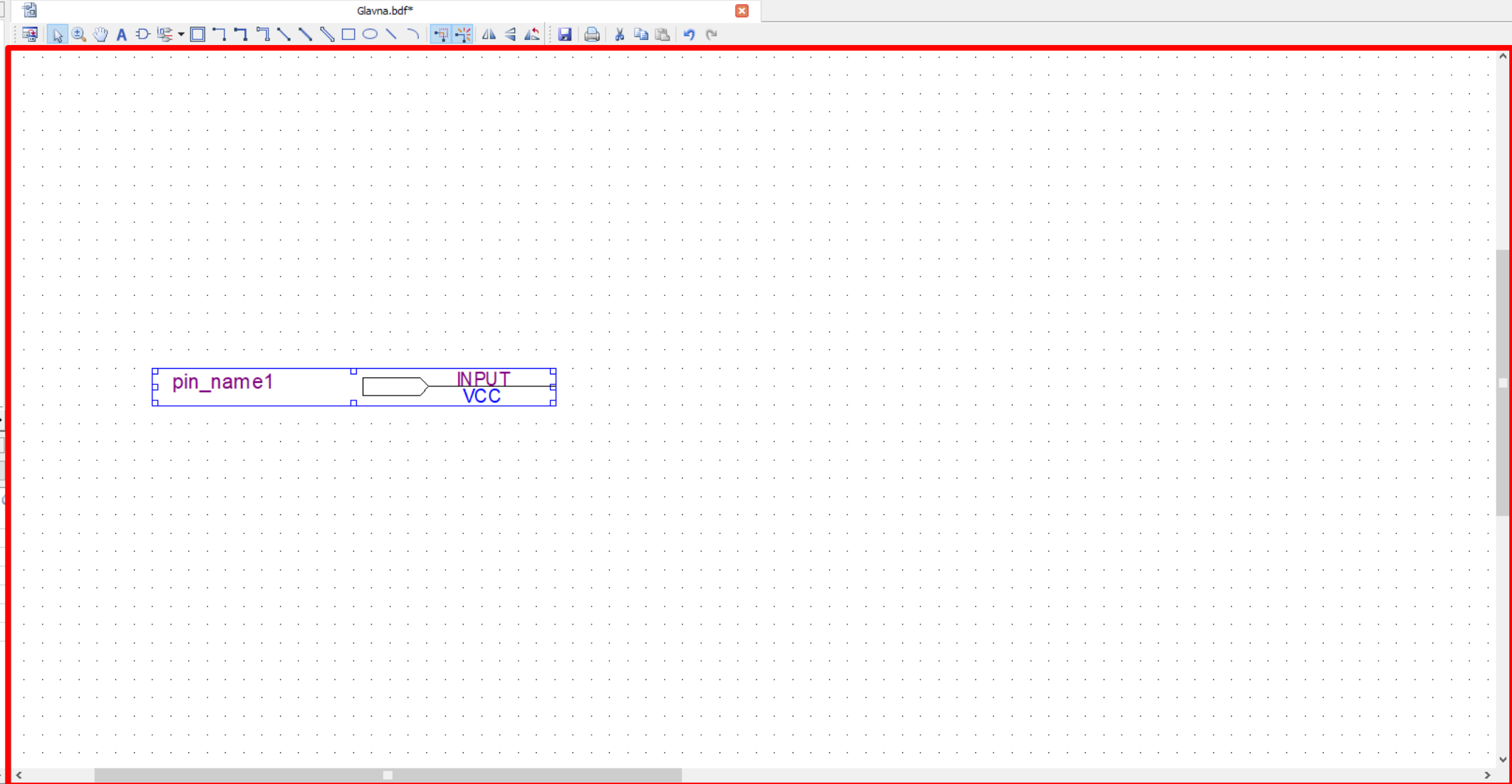




Project Navigator

Files

- Glavna.bdf



Hierarchy Files Design Units

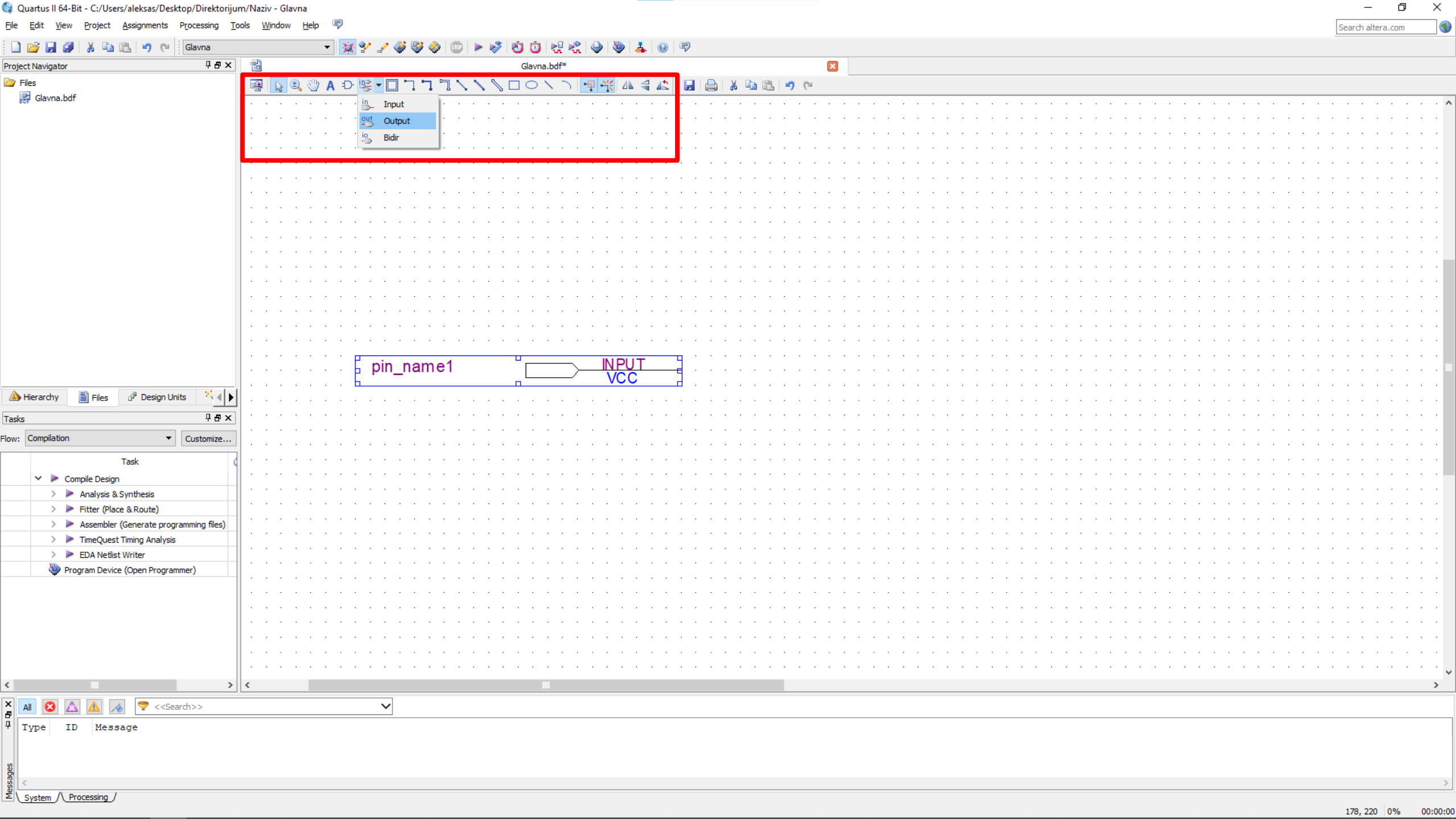
Tasks

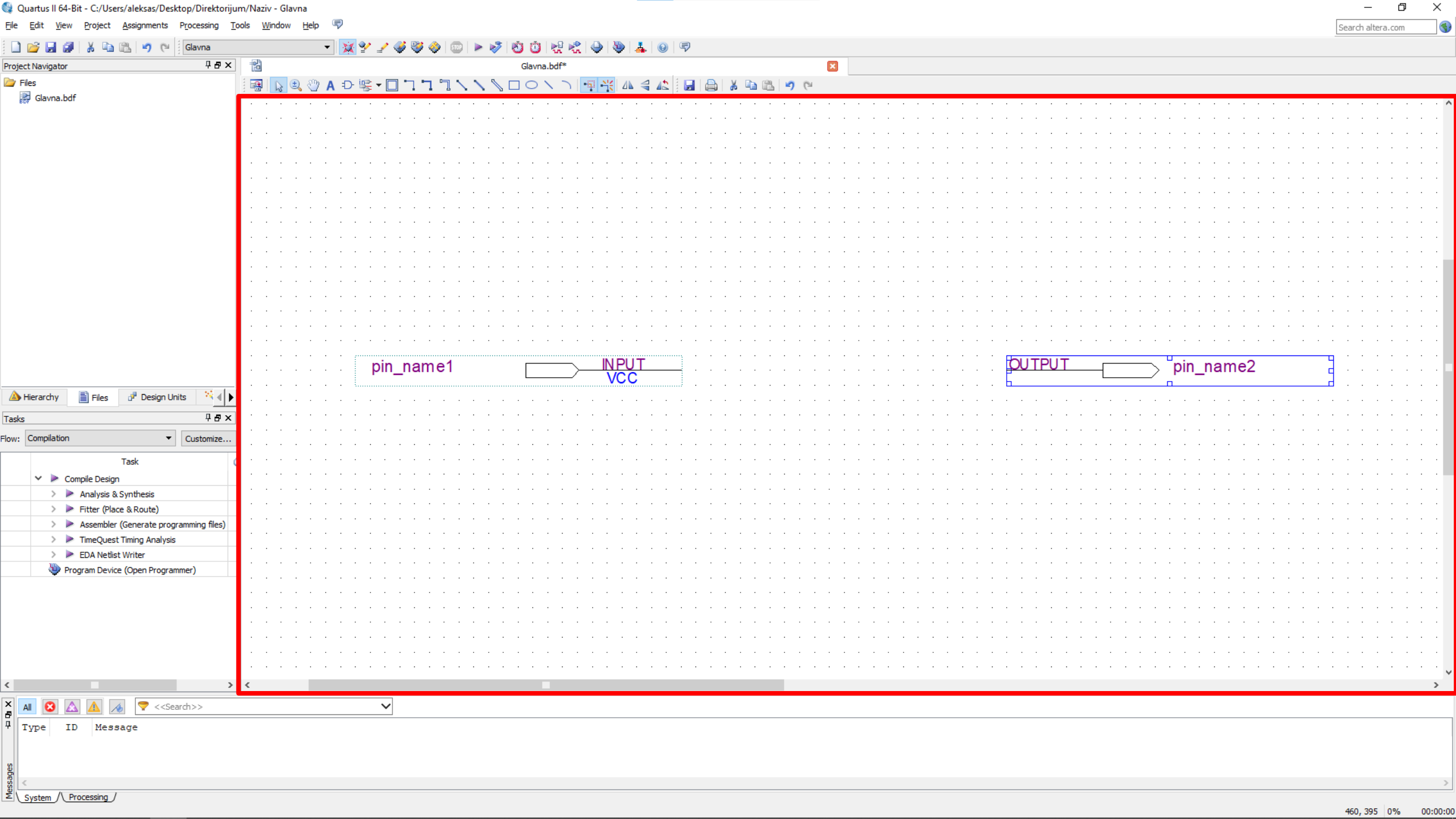
Flow: Compilation Customize...

- Task
- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Programmer)

All [Icons] <<Search>>

Type	ID	Message





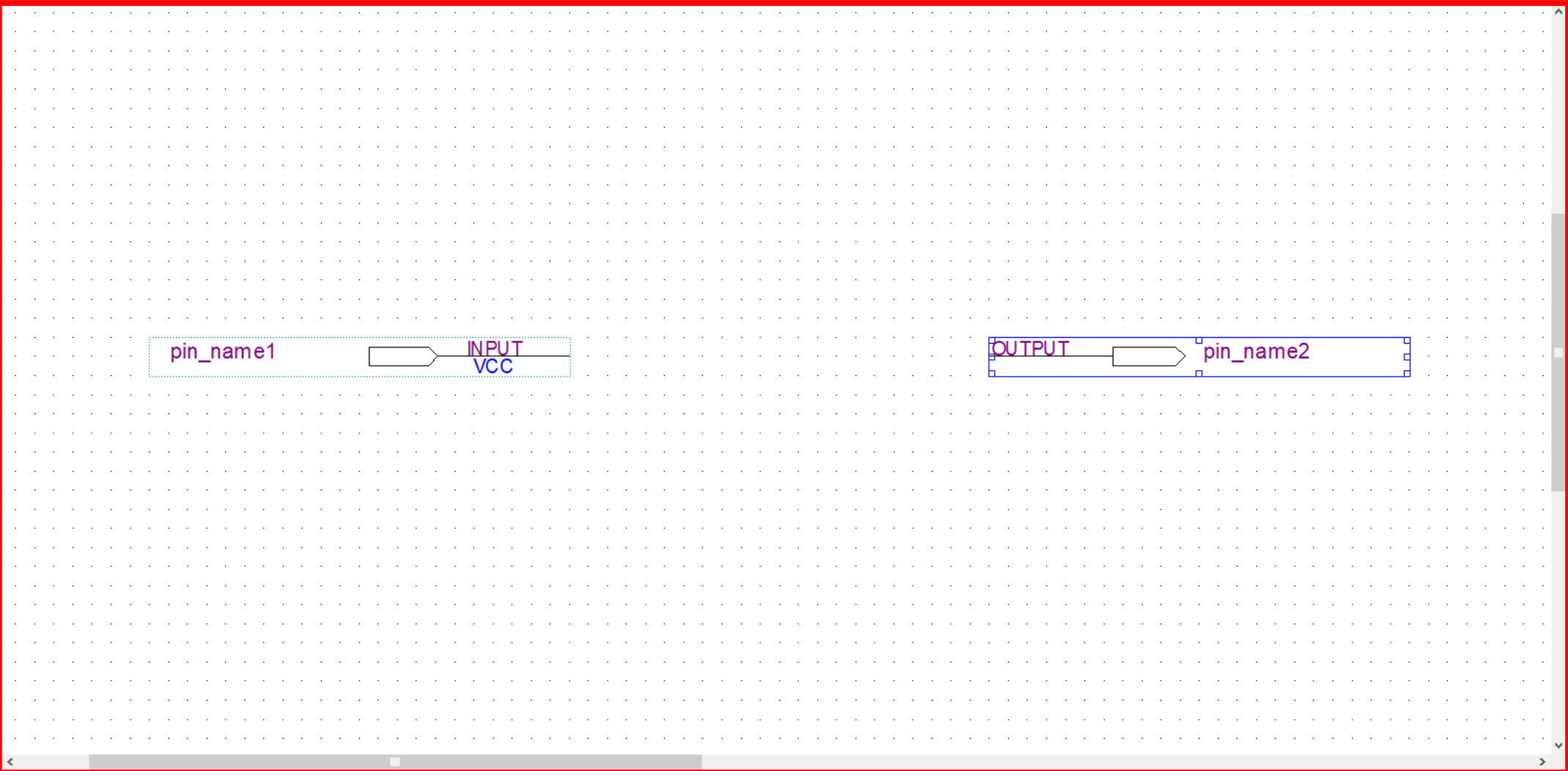
Project Navigator

Files

- Glavna.bdf

Glavna.bdf\*

Glavna



Hierarchy

Files

Design Units

Tasks

Flow: Compilation

Customize...

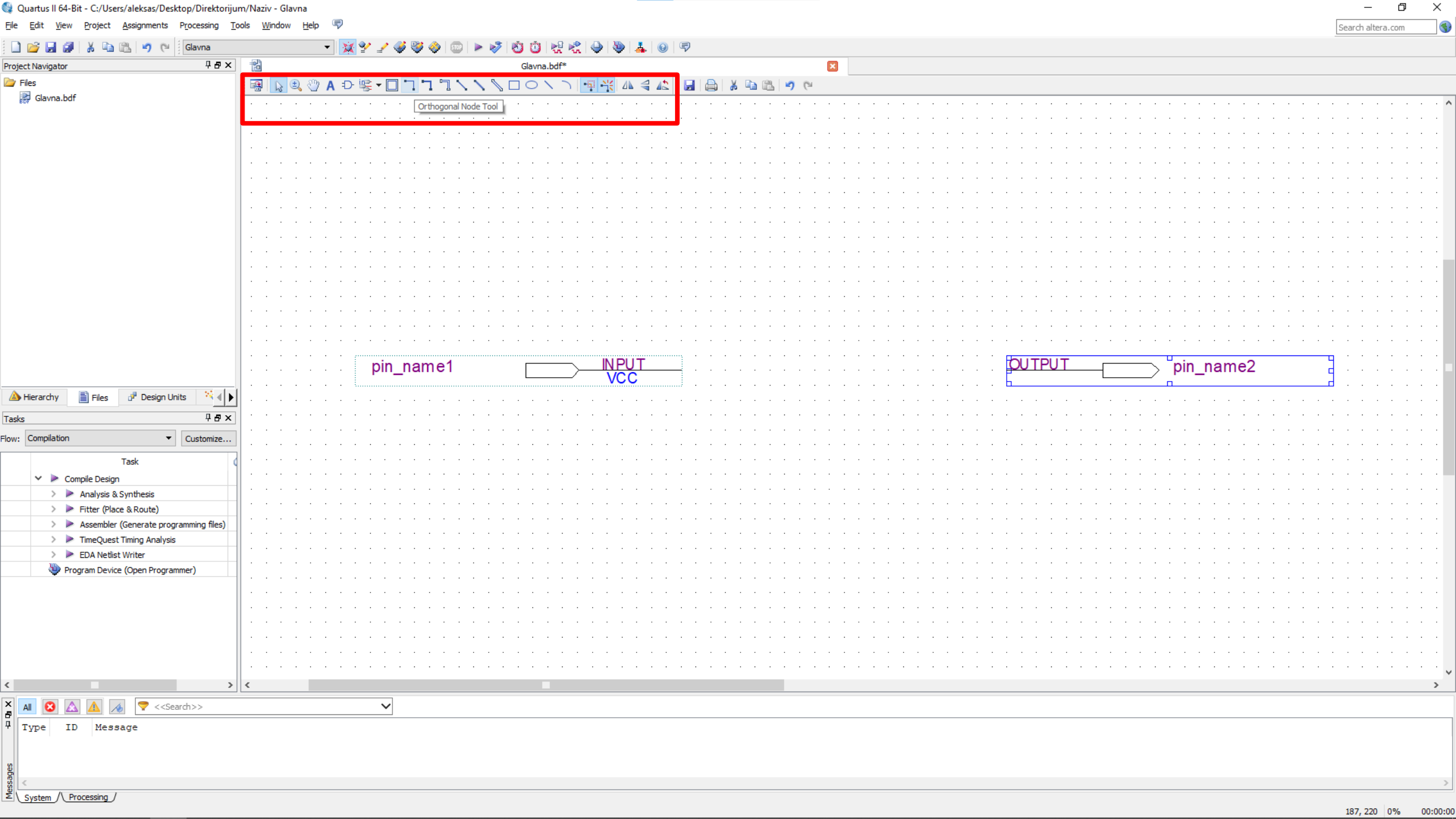
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    - Assembler (Generate programming files)
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    - EDA Netlist Writer
    - Program Device (Open Programmer)

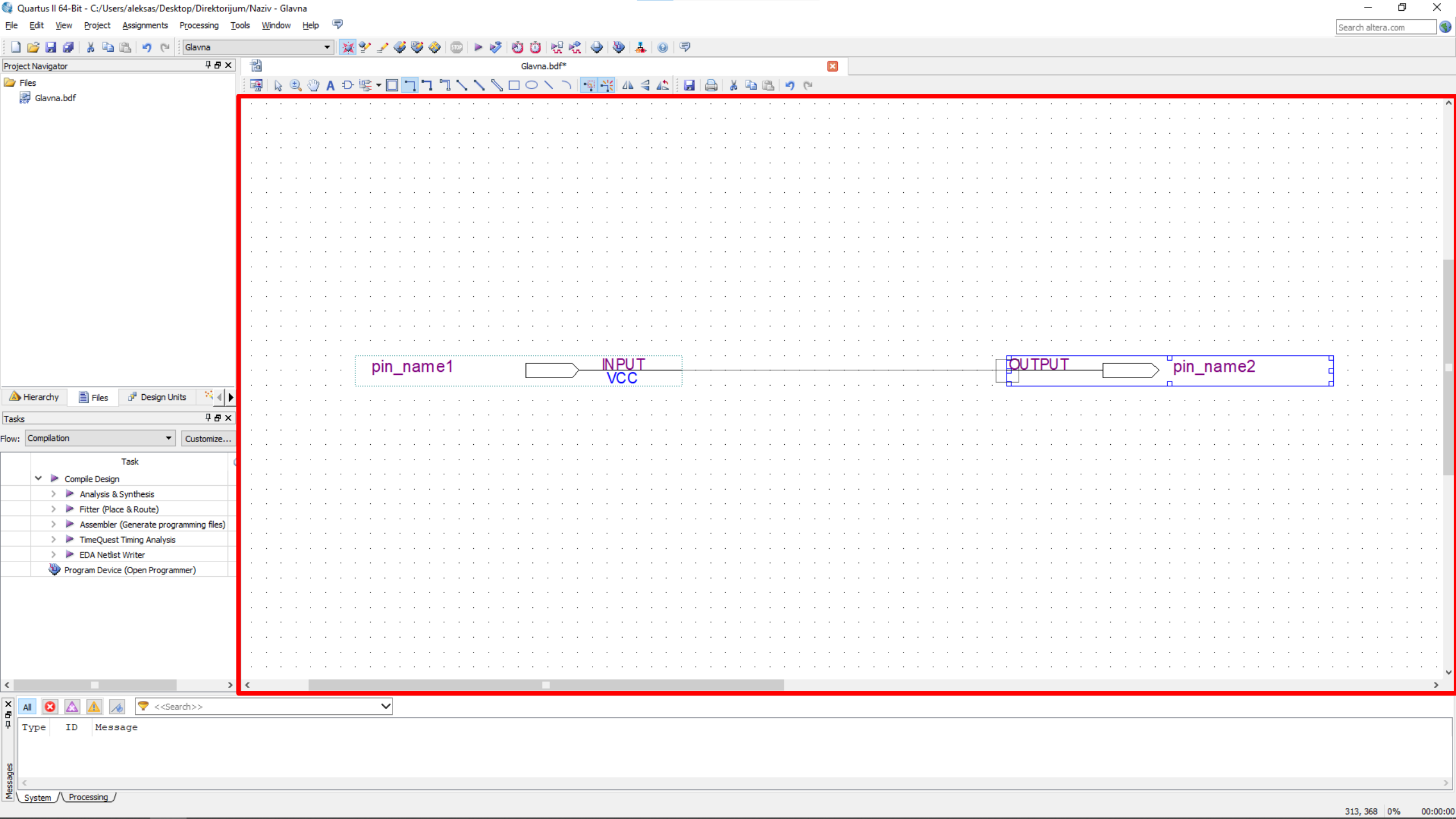
All

<<Search>>

Type	ID	Message

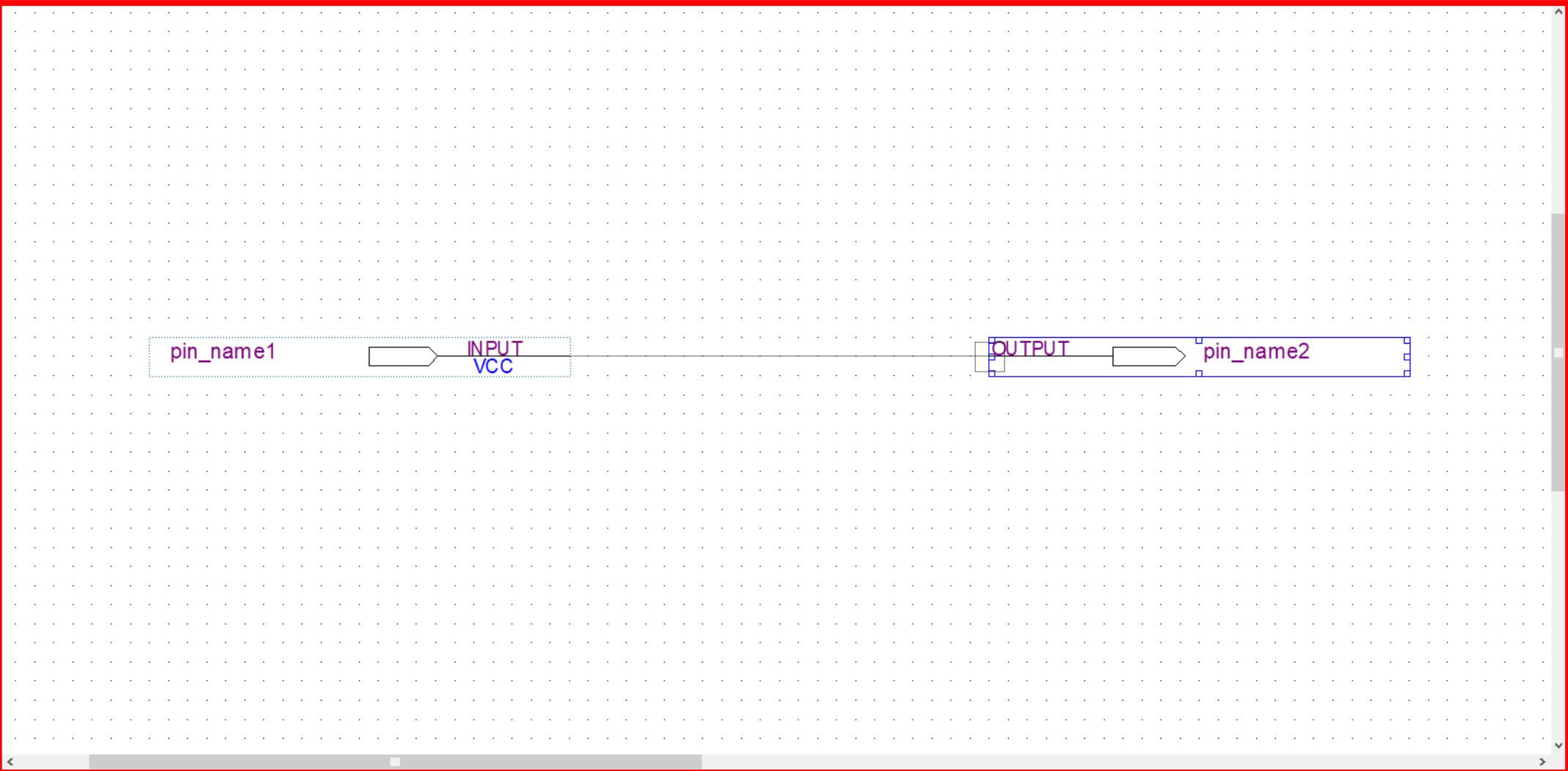
System / Processing





Project Navigator  
Files  
Glavna.bdf

Glavna.bdf\*  
[Toolbars: Selection, Drawing, Editing, etc.]



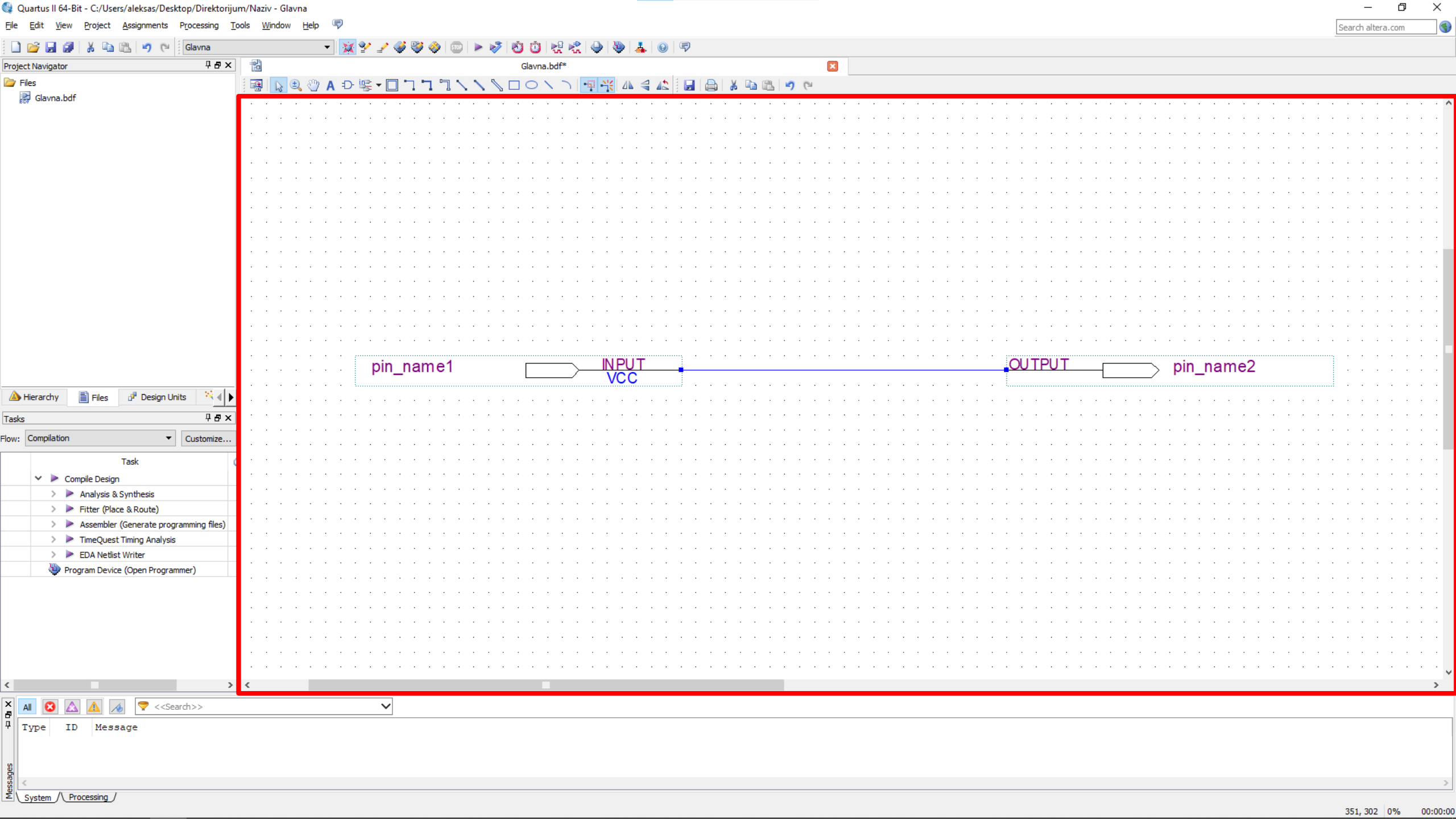
Hierarchy Files Design Units

Tasks  
Flow: Compilation Customize...

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All [Icons] <<Search>>

Type	ID	Message
System		Processing

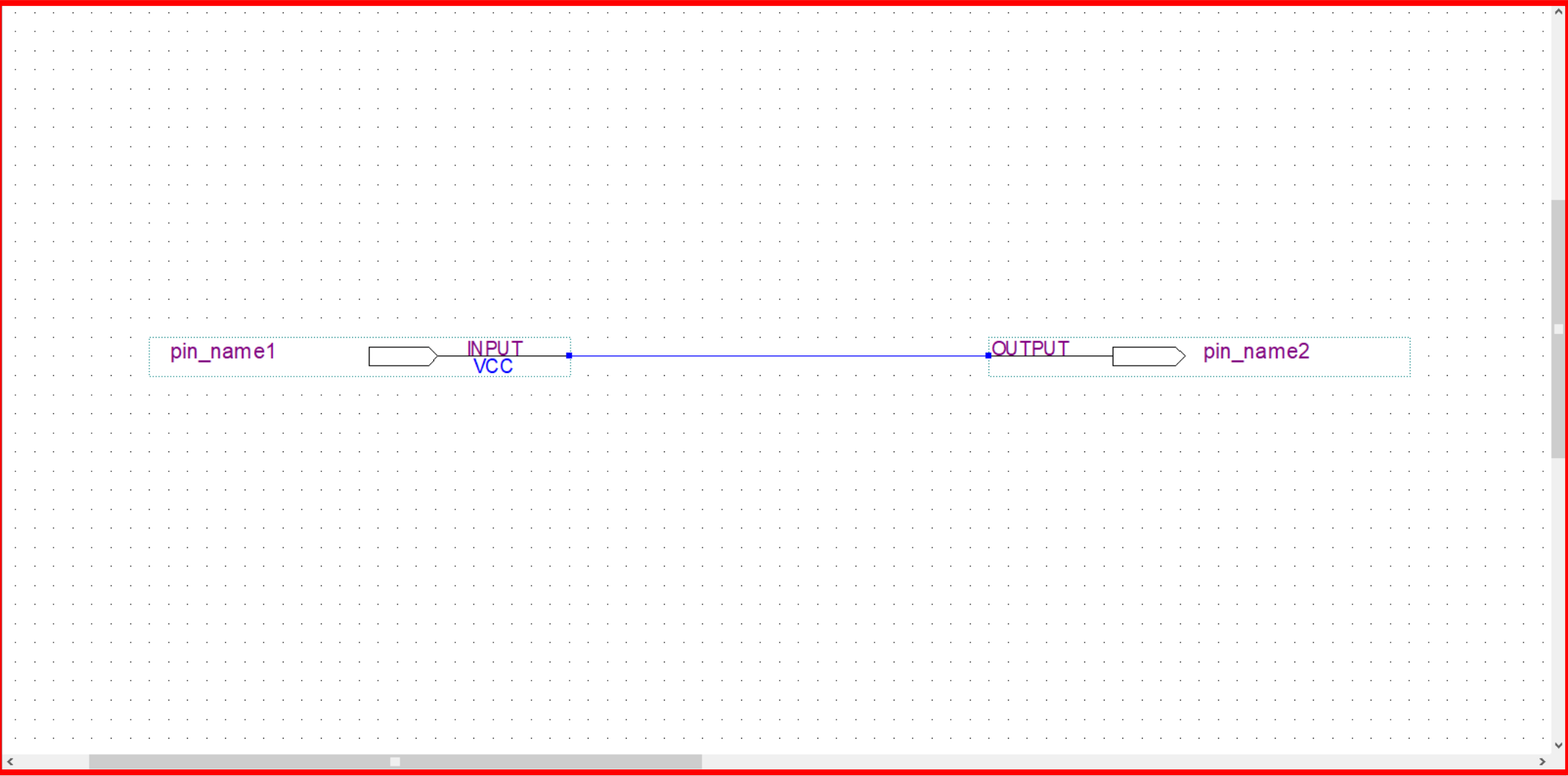


Project Navigator  
Files  
Glavna.bdf

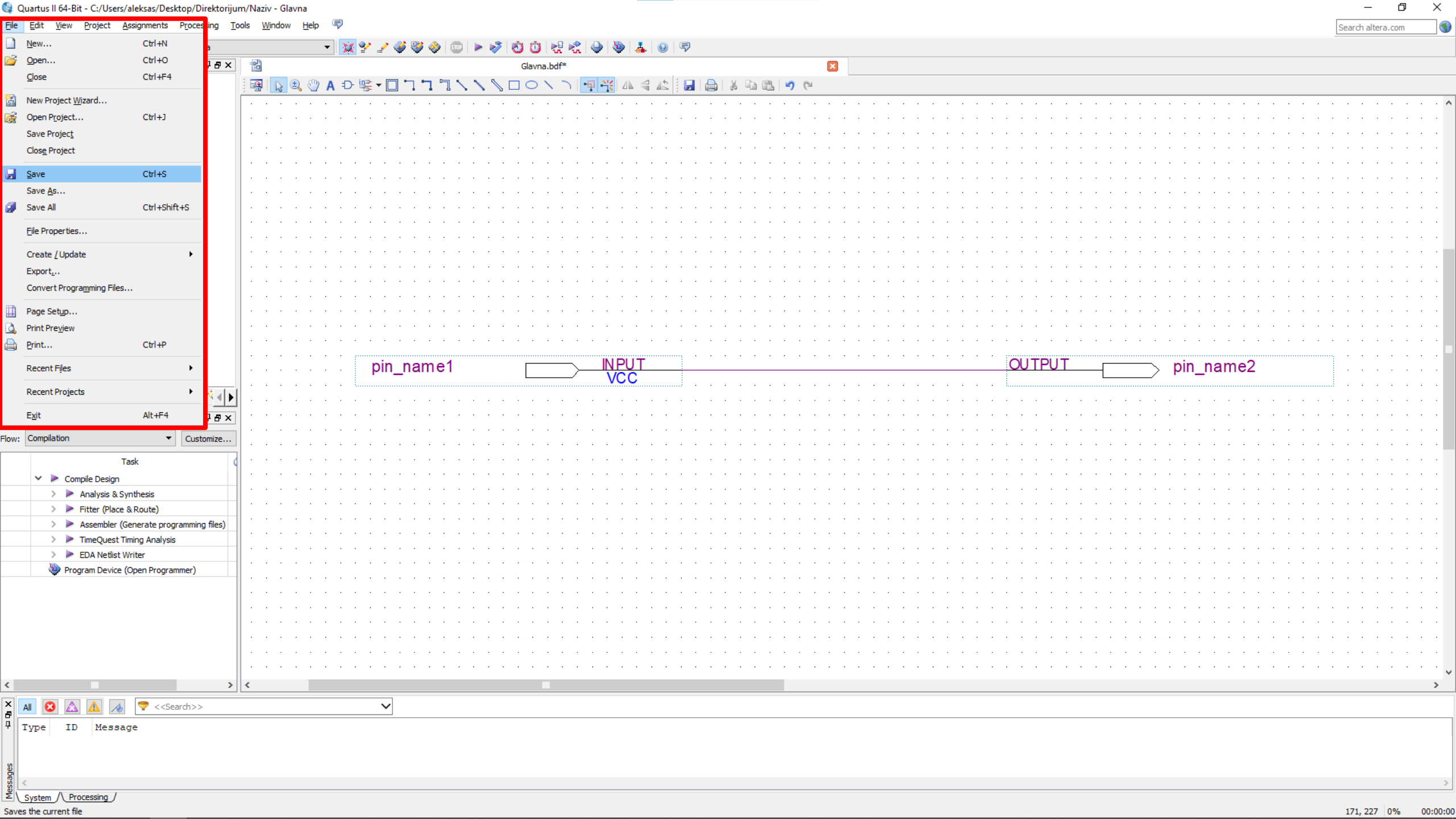
Glavna.bdf\*

Hierarchy Files Design Units

Tasks  
Flow: Compilation  
Task  
Compile Design  
Analysis & Synthesis  
Fitter (Place & Route)  
Assembler (Generate programming files)  
TimeQuest Timing Analysis  
EDA Netlist Writer  
Program Device (Open Programmer)



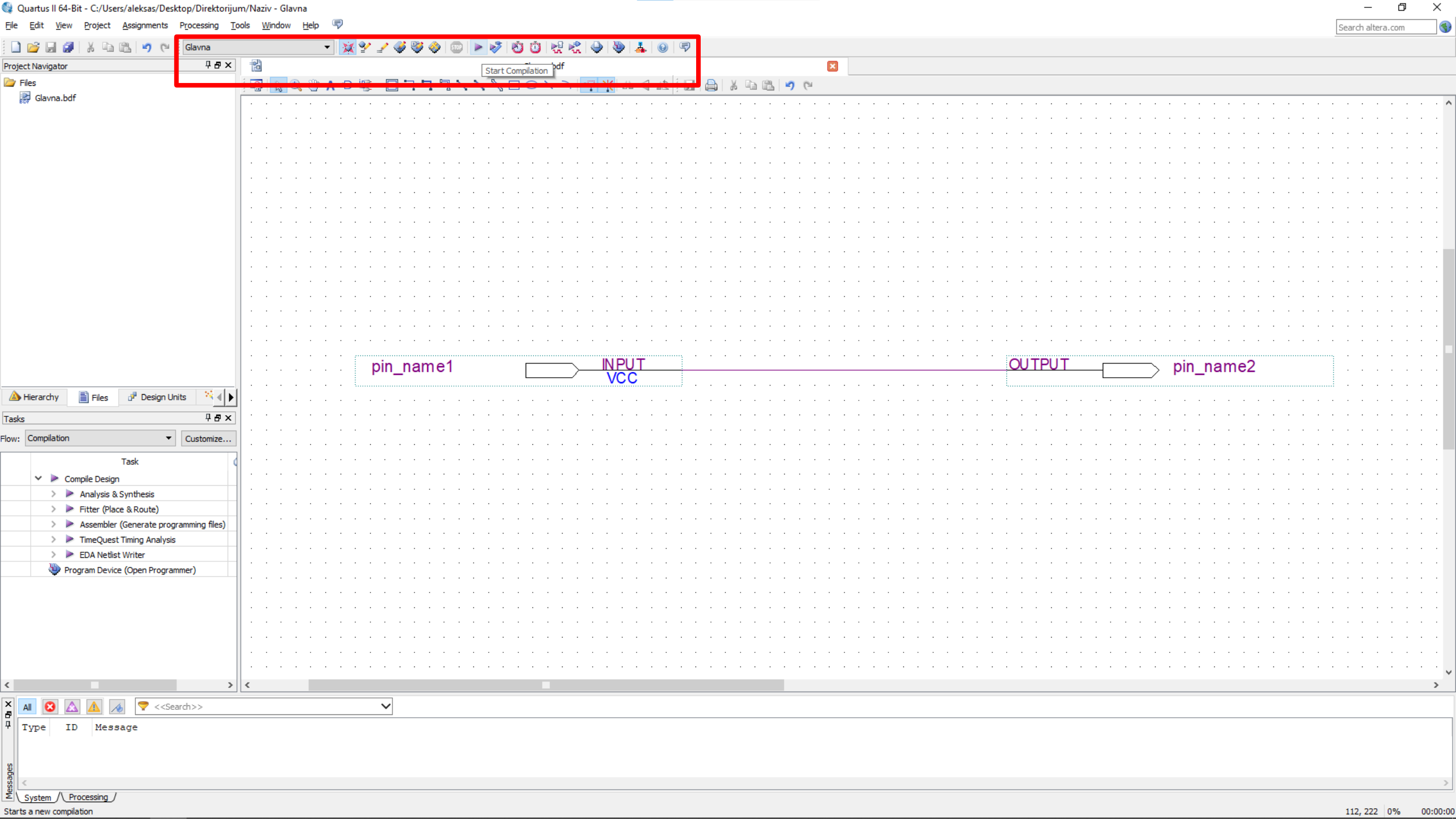
Messages  
All [Icons] <<Search>>  
Type ID Message  
System Processing



# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device (Open Programmer)
- Add File...
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- Start





Glavna

Start Compilation pdf

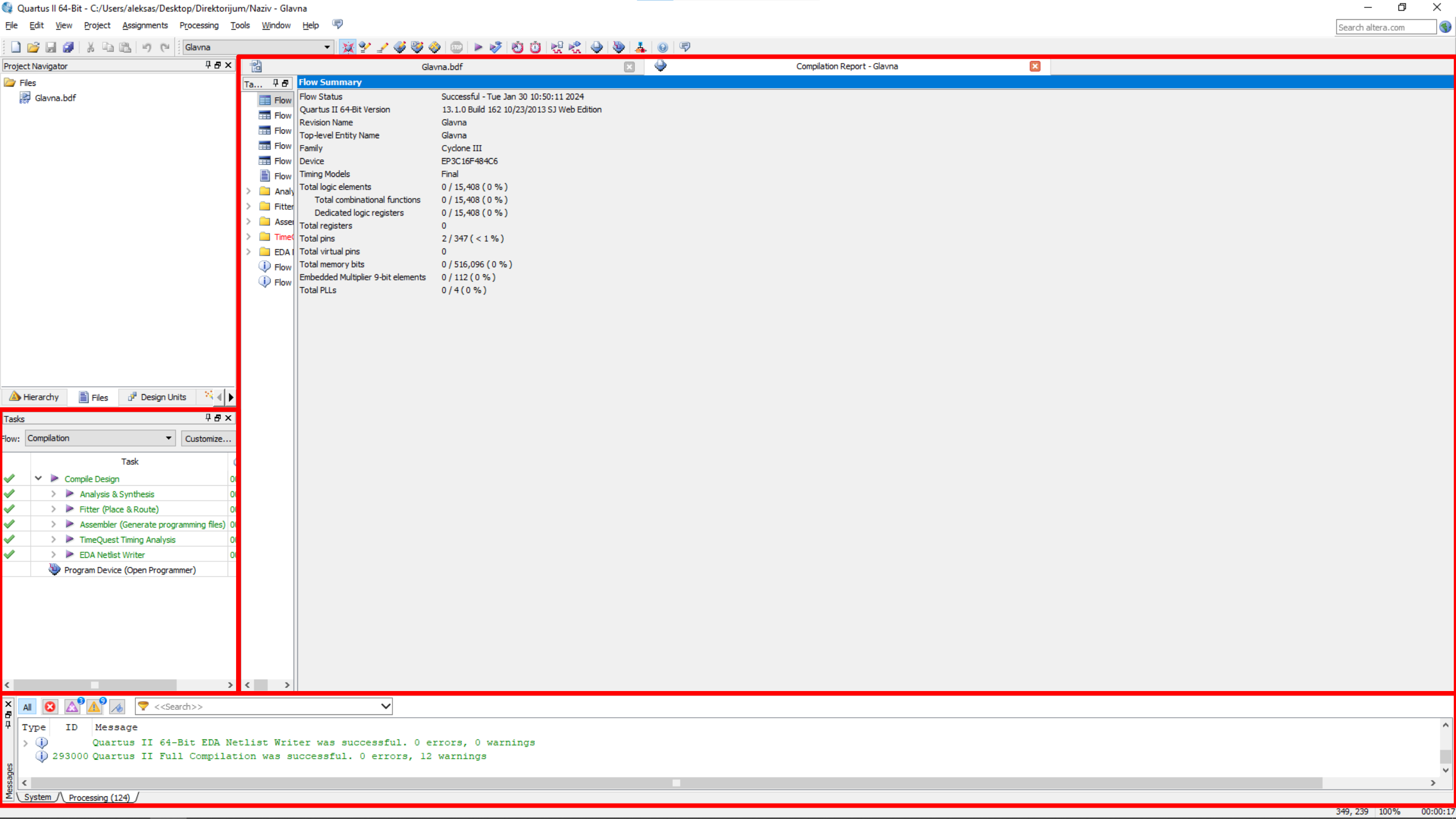


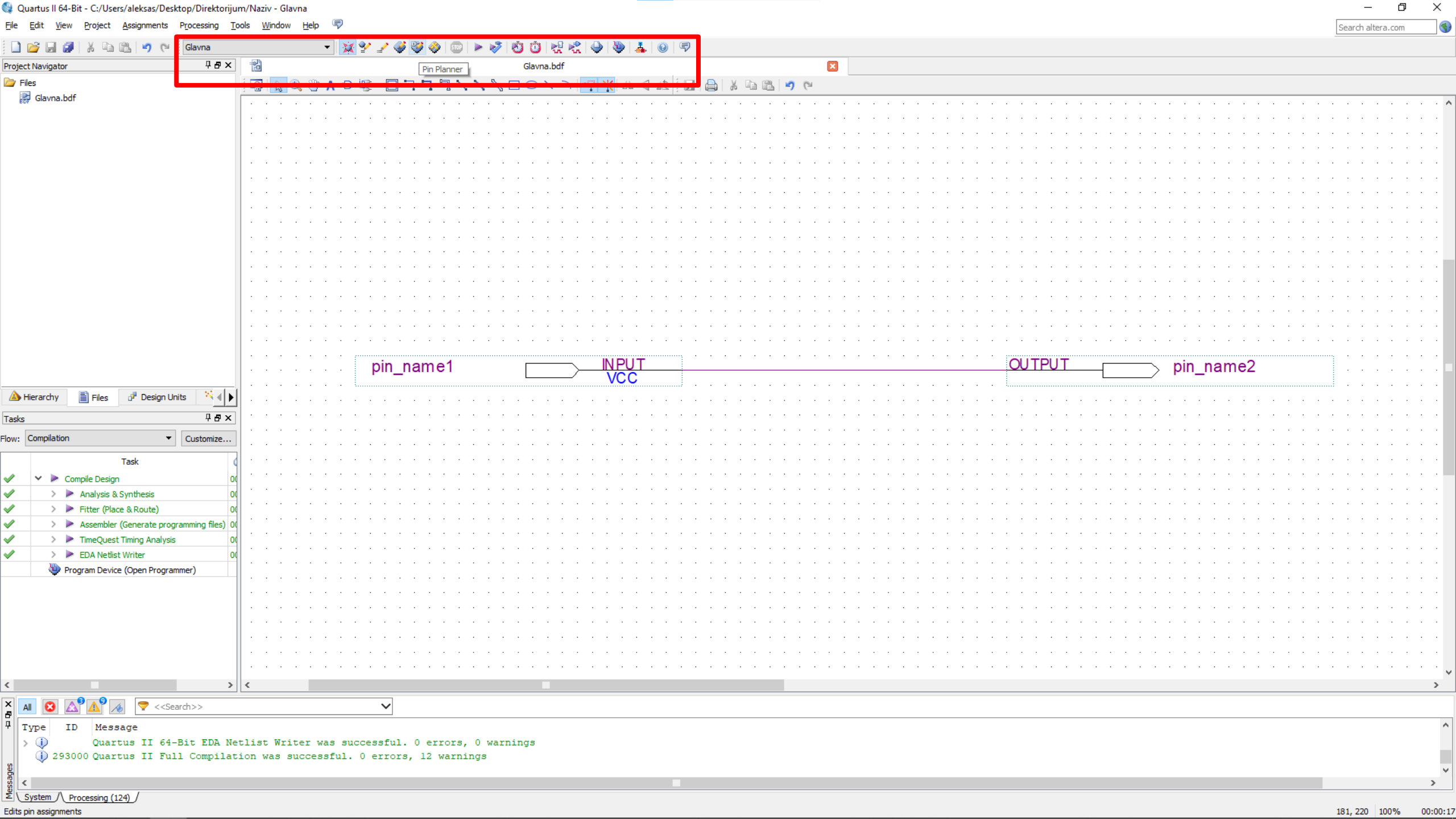
- Tasks
- Flow: Compilation Customize...
- Task
  - Compile Design
    - Analysis & Synthesis
    - Fitter (Place & Route)
    - Assembler (Generate programming files)
    - TimeQuest Timing Analysis
    - EDA Netlist Writer
    - Program Device (Open Programmer)

Messages

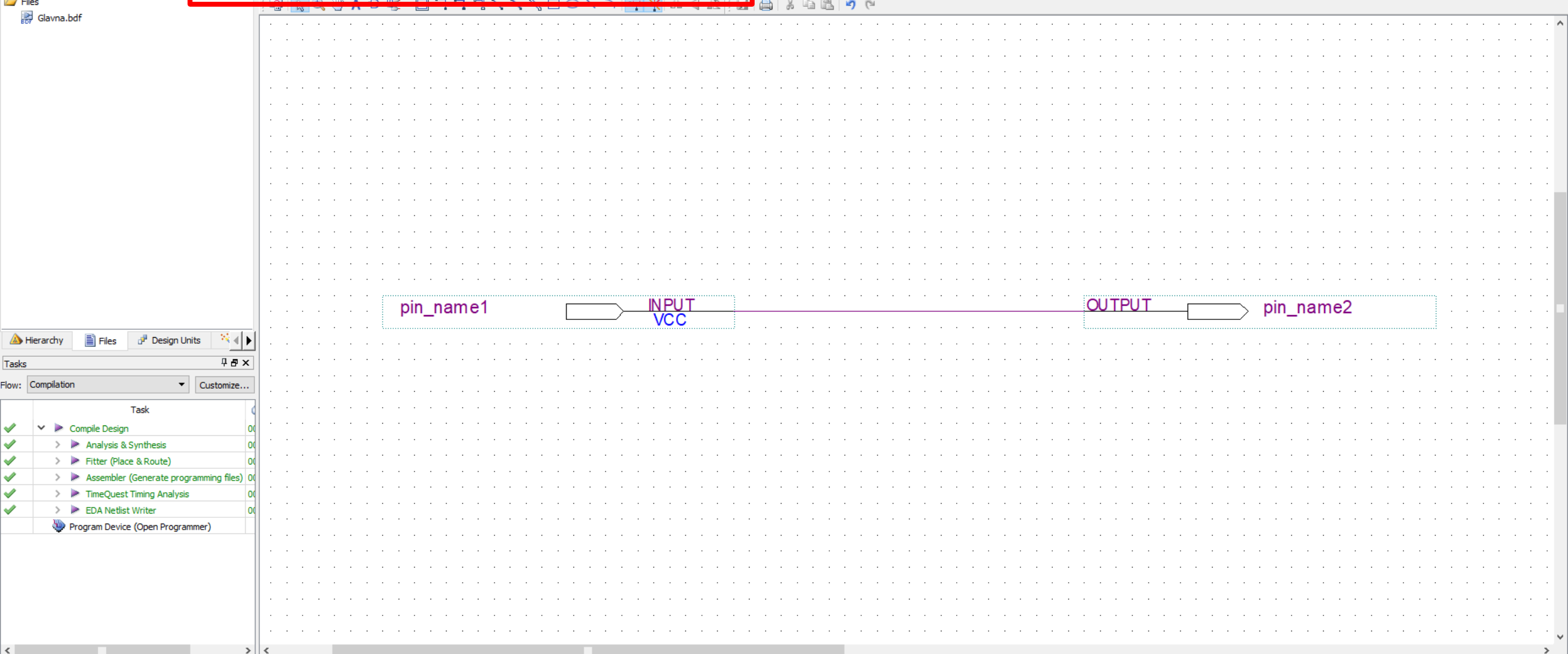
All [Icons] <<Search>>

Type	ID	Message
System	Processing	Starts a new compilation





Project Navigator: Glavna, Glavna.bdf



Tasks: Compilation

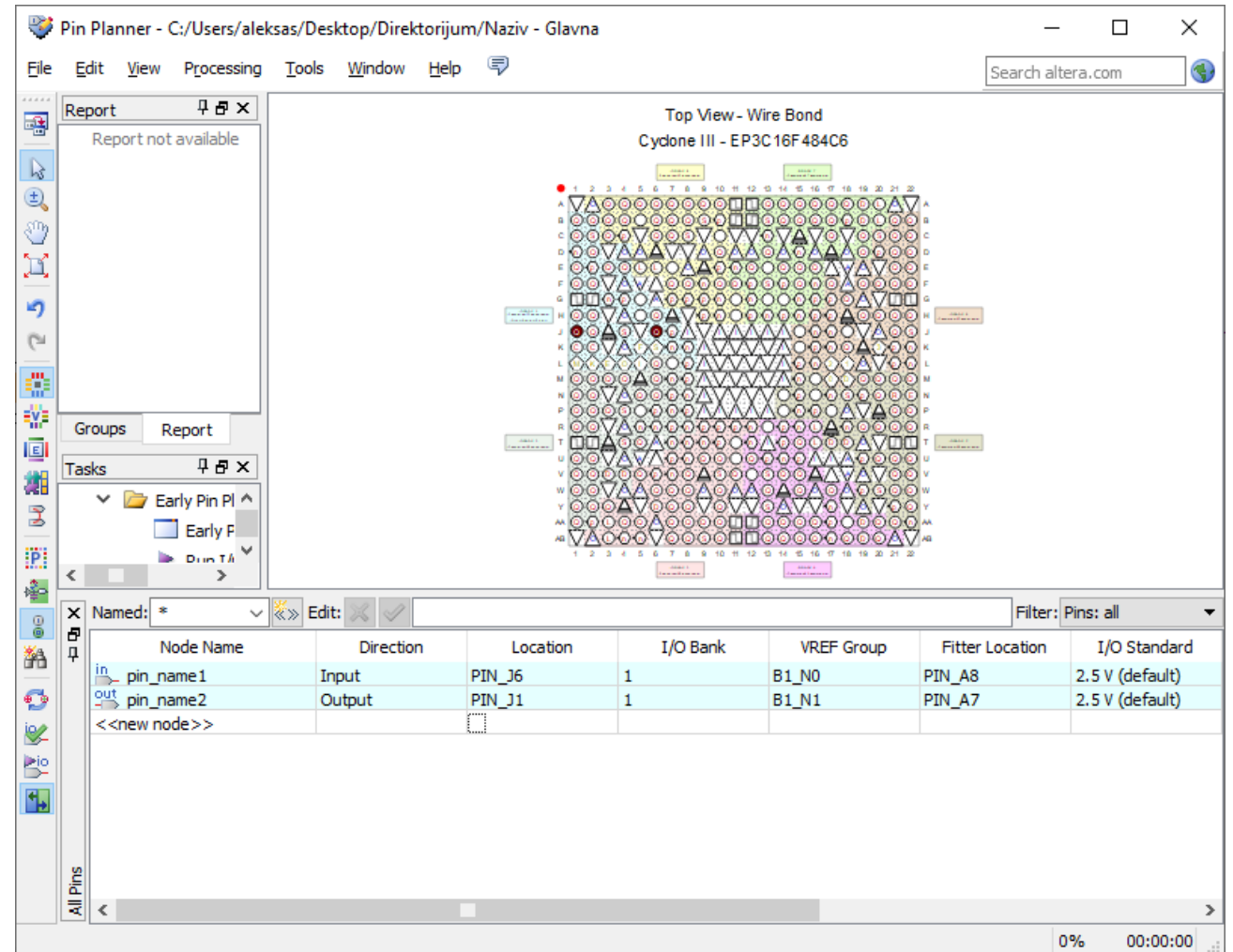
Task	Progress
Compile Design	00%
Analysis & Synthesis	00%
Fitter (Place & Route)	00%
Assembler (Generate programming files)	00%
TimeQuest Timing Analysis	00%
EDA Netlist Writer	00%
Program Device (Open Programmer)	

Messages

Type	ID	Message
Info		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 12 warnings

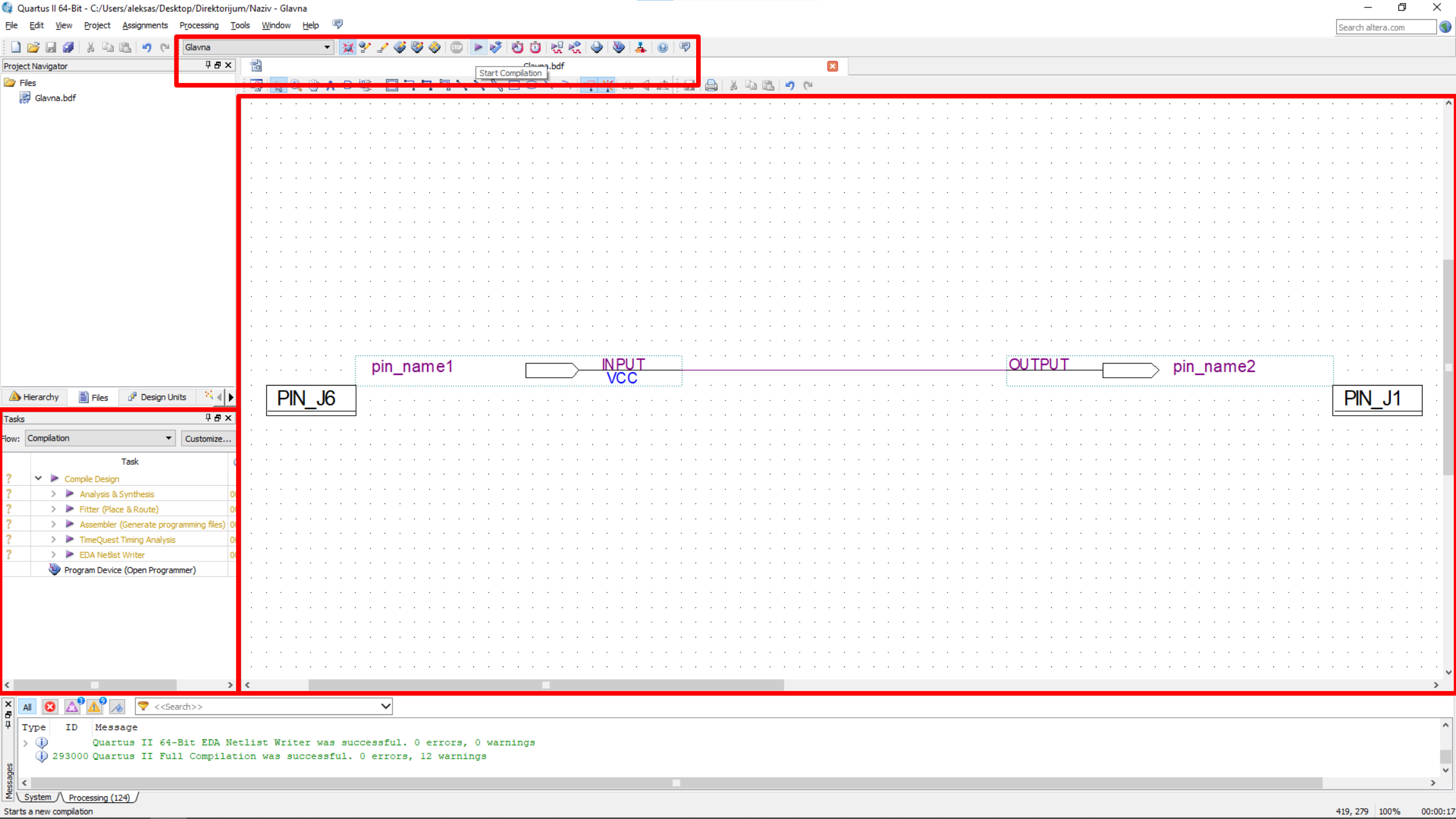
# Спуштање шеме на плочицу

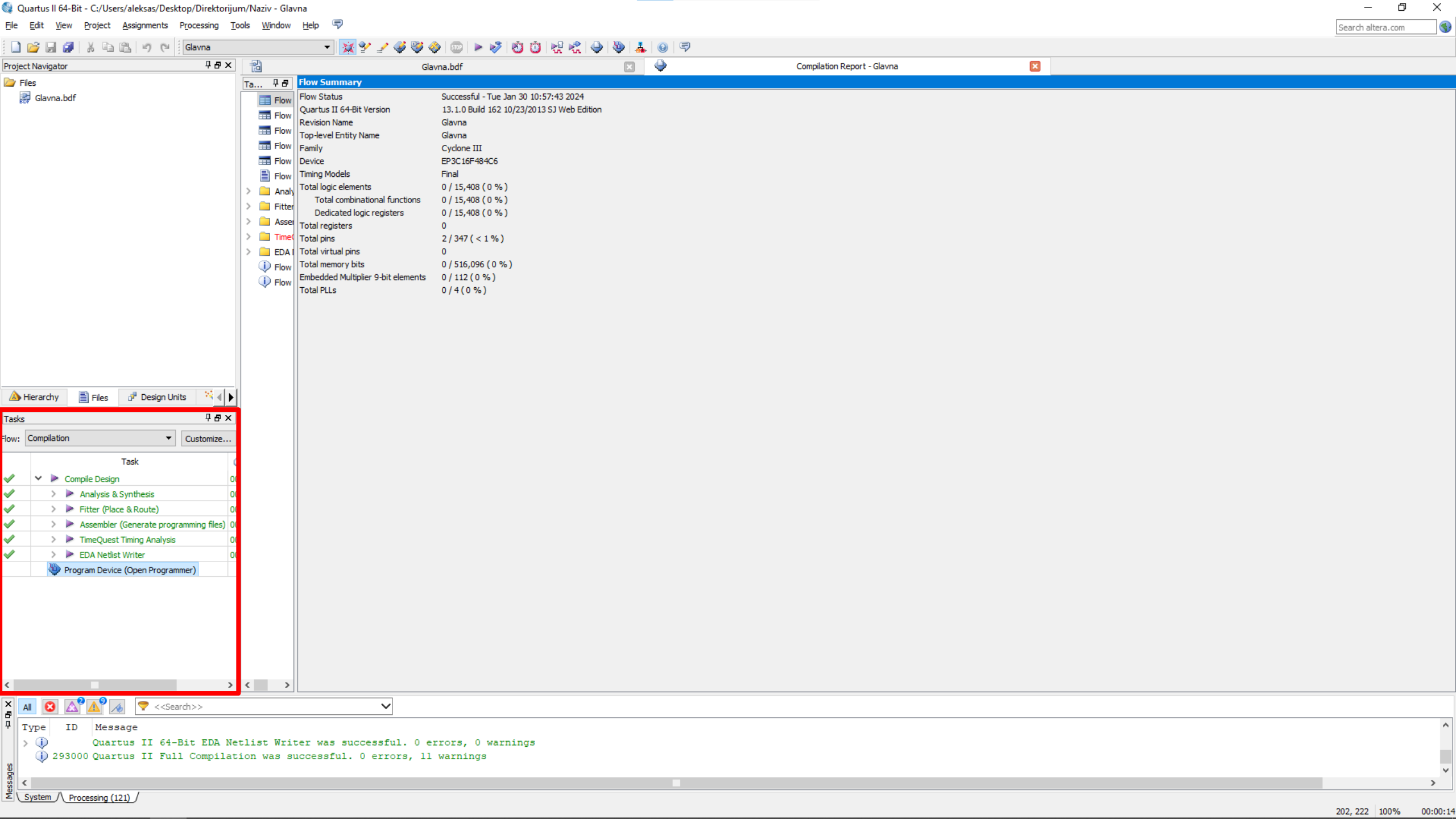
- Standard -> Start Compilation
- Standard -> Pin Planner
- **Location -> Close**
- Standard -> Start Compilation
- Tasks -> Program Device (Open Programmer)
- Add File...
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- Start



The screenshot displays the Pin Planner application window. The main area shows a top view of the Cyclone III EP3C16F484C6 chip with a grid of pins. The interface includes a menu bar (File, Edit, View, Processing, Tools, Window, Help), a search bar, and several toolbars. A 'Report' window is open on the left, showing 'Report not available'. The 'Tasks' window shows a tree view with 'Early Pin Pl' and 'Early P'. The 'All Pins' window at the bottom displays a table of pin configurations.

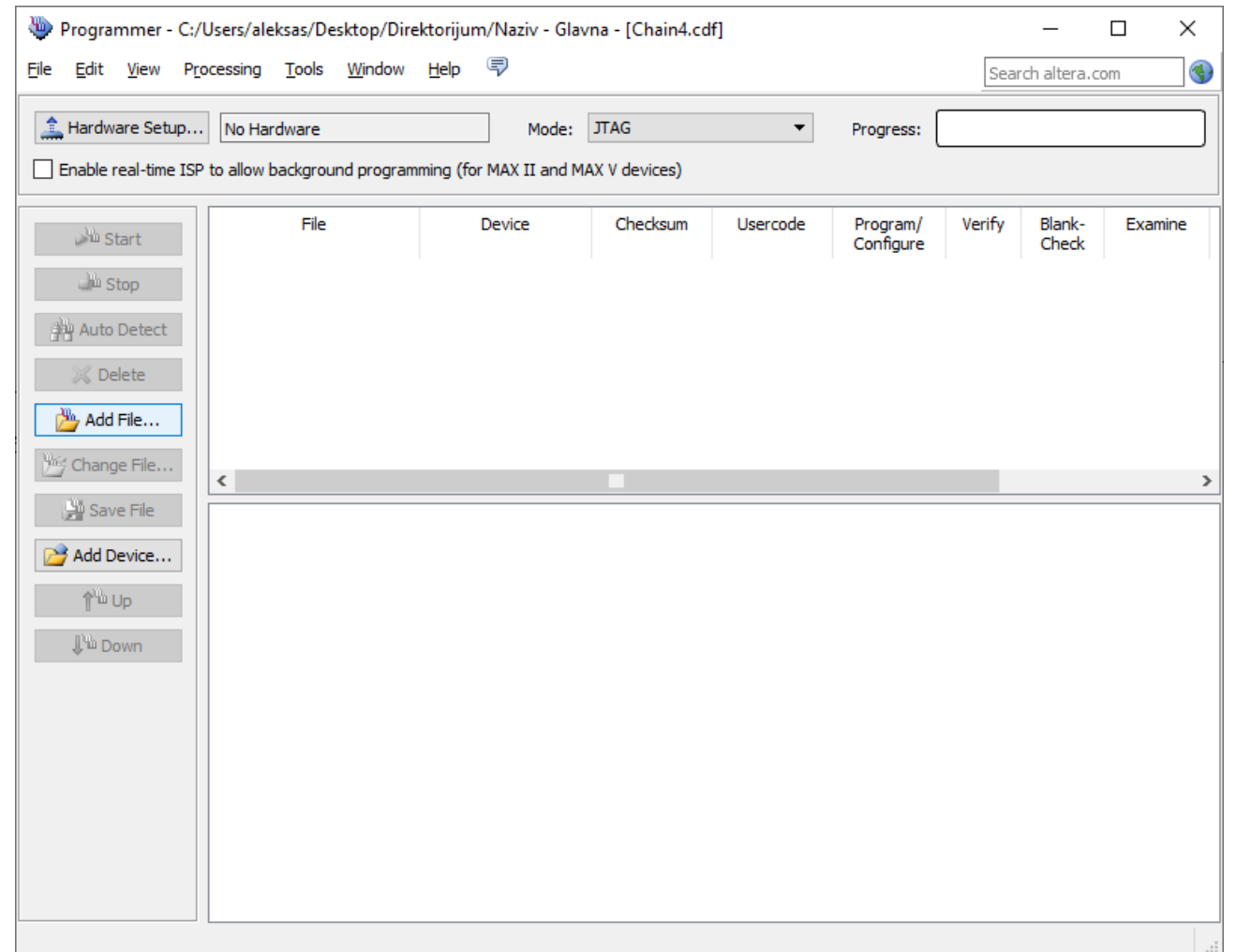
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in pin_name1	Input	PIN_J6	1	B1_N0	PIN_A8	2.5 V (default)
out pin_name2	Output	PIN_J1	1	B1_N1	PIN_A7	2.5 V (default)
<<new node>>						





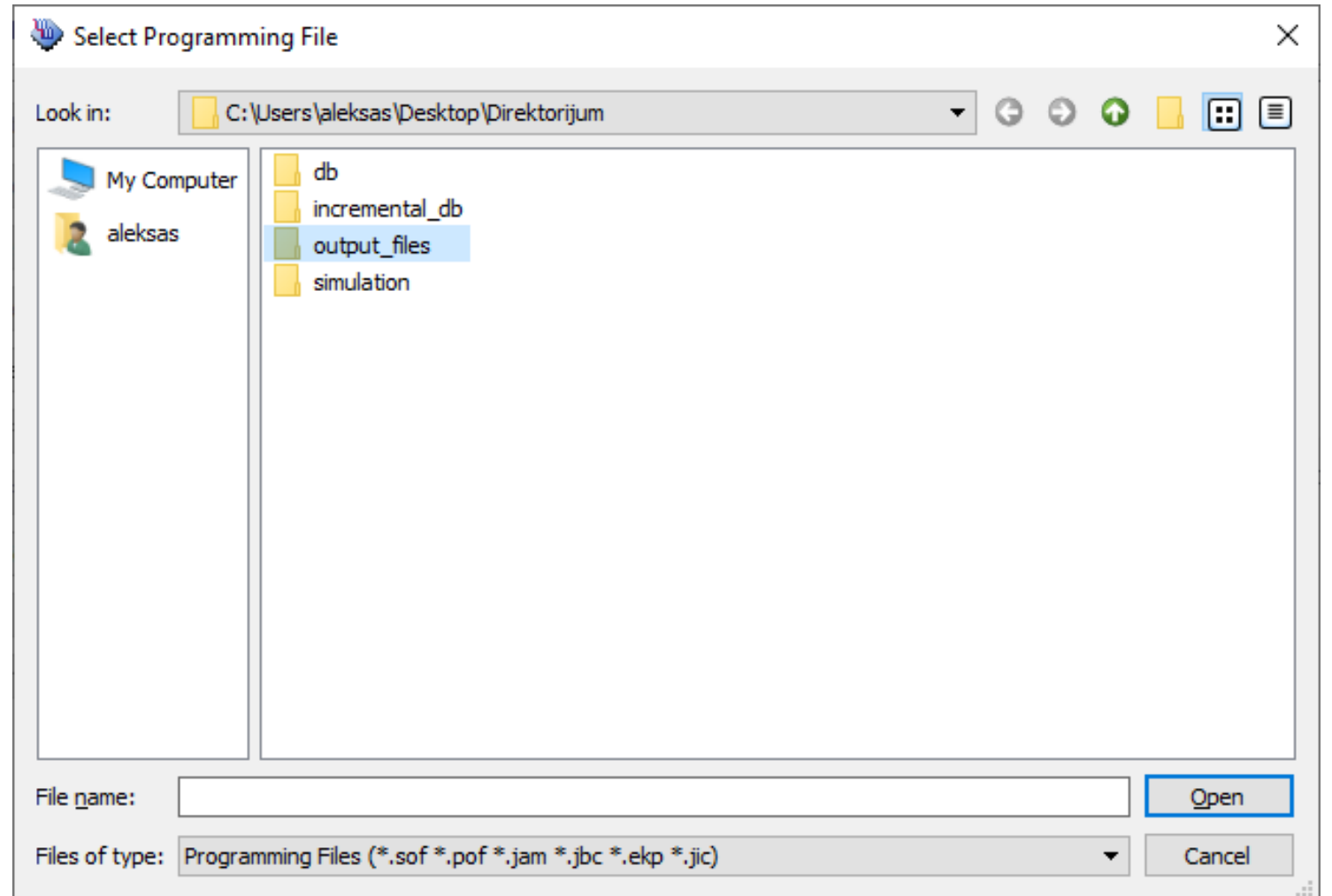
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- **Add File...**
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- Start



# Спуштање шеме на плочицу

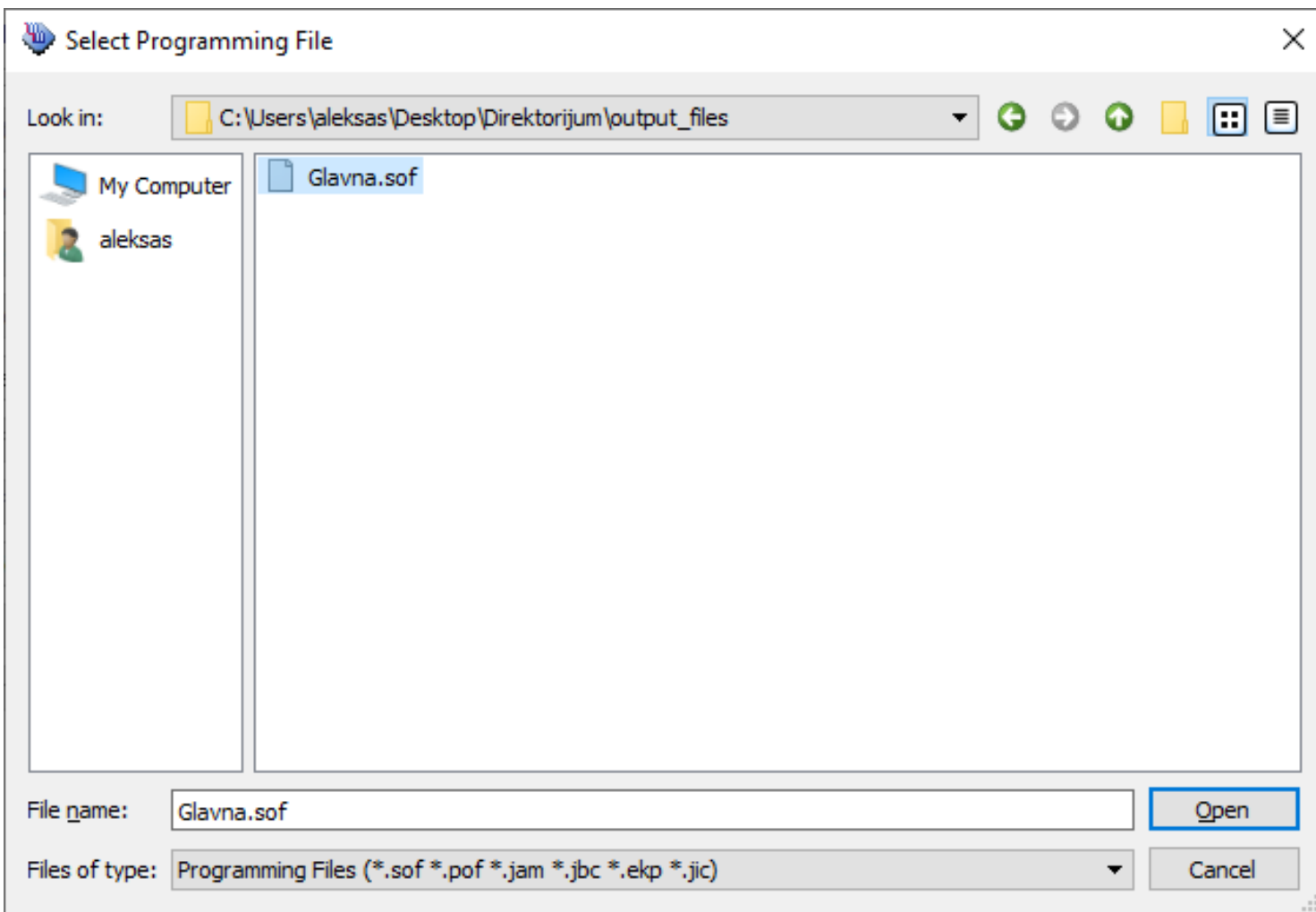
- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- **File Name -> Open**
- Hardware Setup...
- Currently Selected Hardware -> Close
- Start





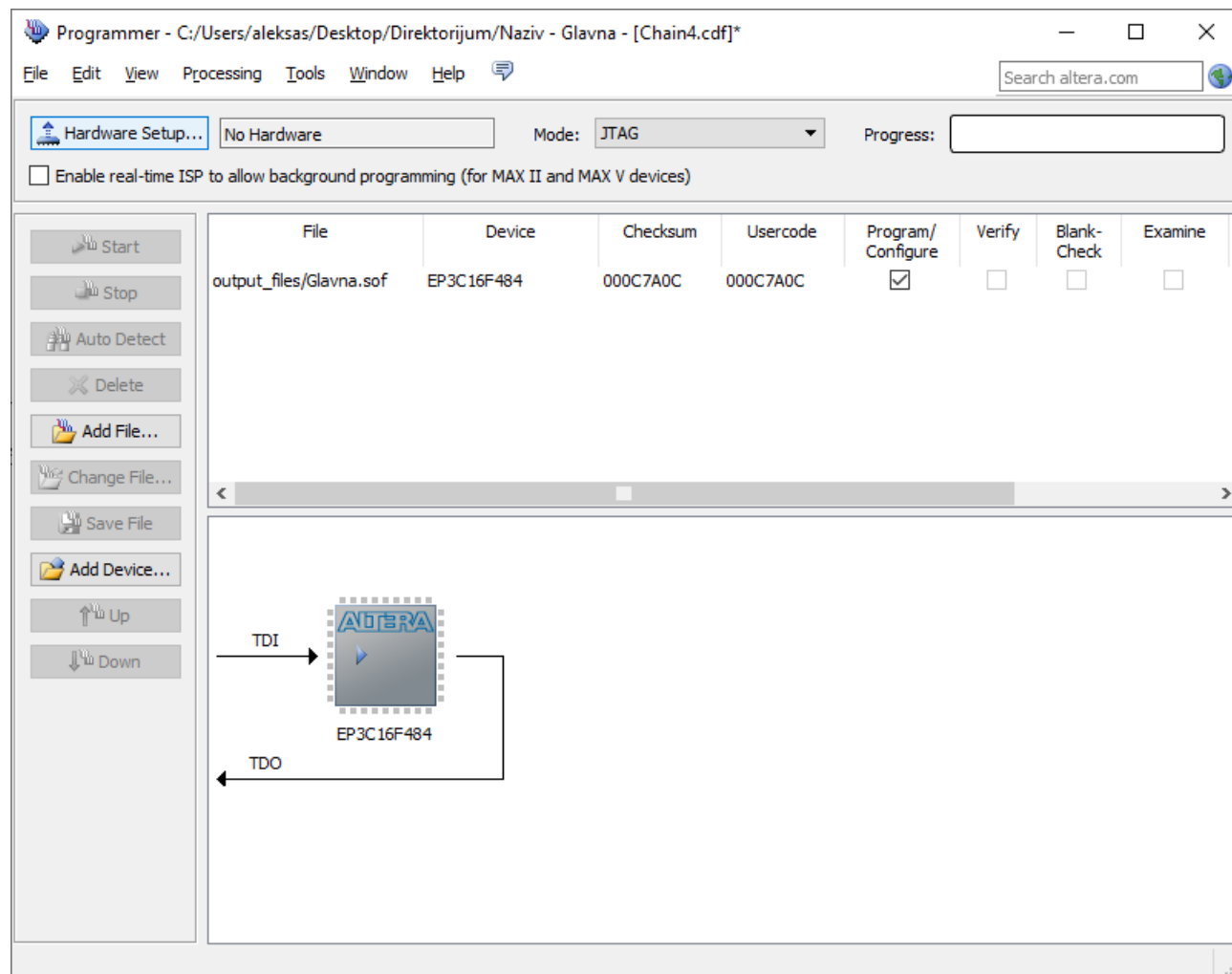
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- **File Name -> Open**
- Hardware Setup...
- Currently Selected Hardware -> Close
- Start



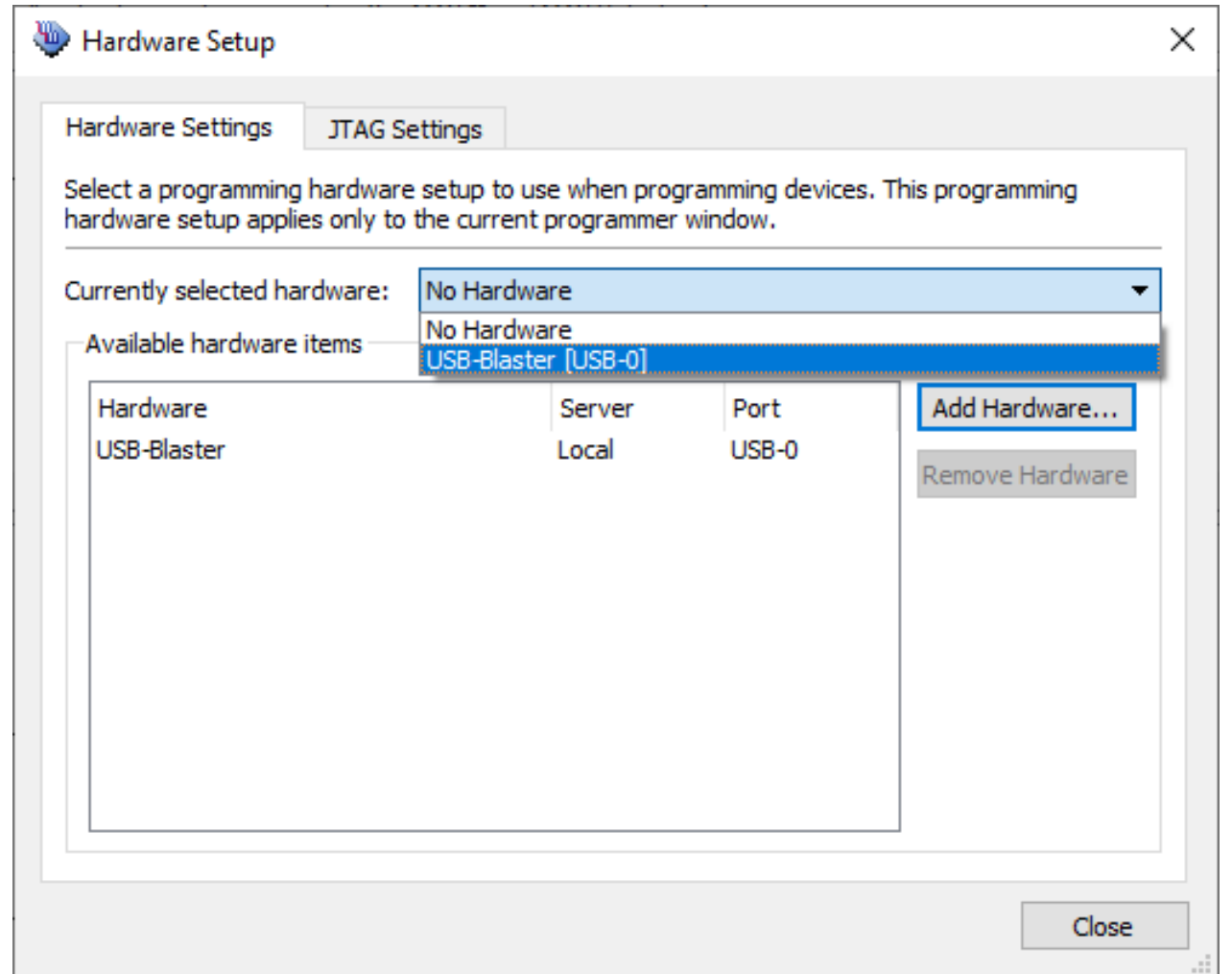
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- **Hardware Setup...**
- Currently Selected Hardware -> Close
- Start



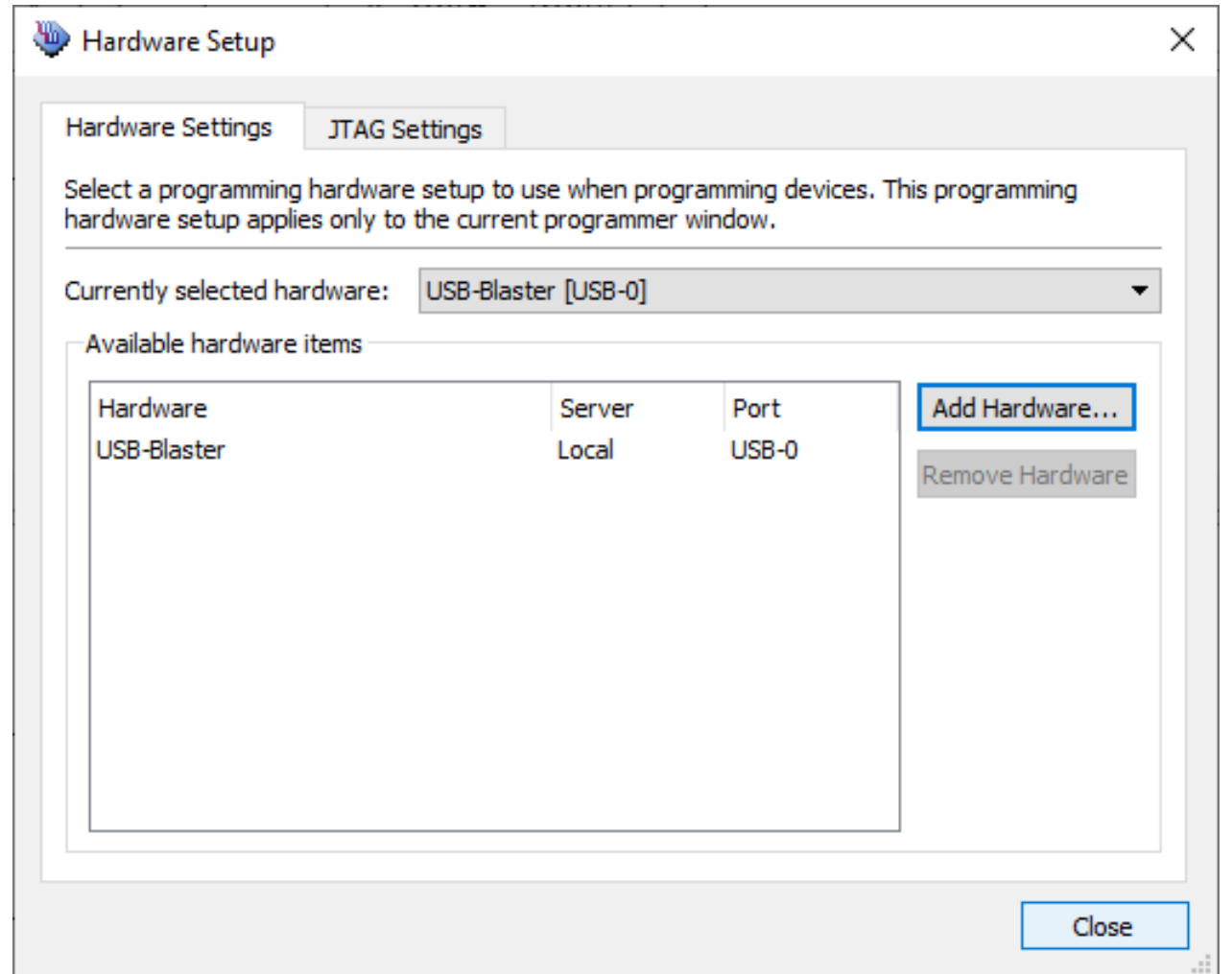
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- Hardware Setup...
- **Currently Selected Hardware -> Close**
- Start



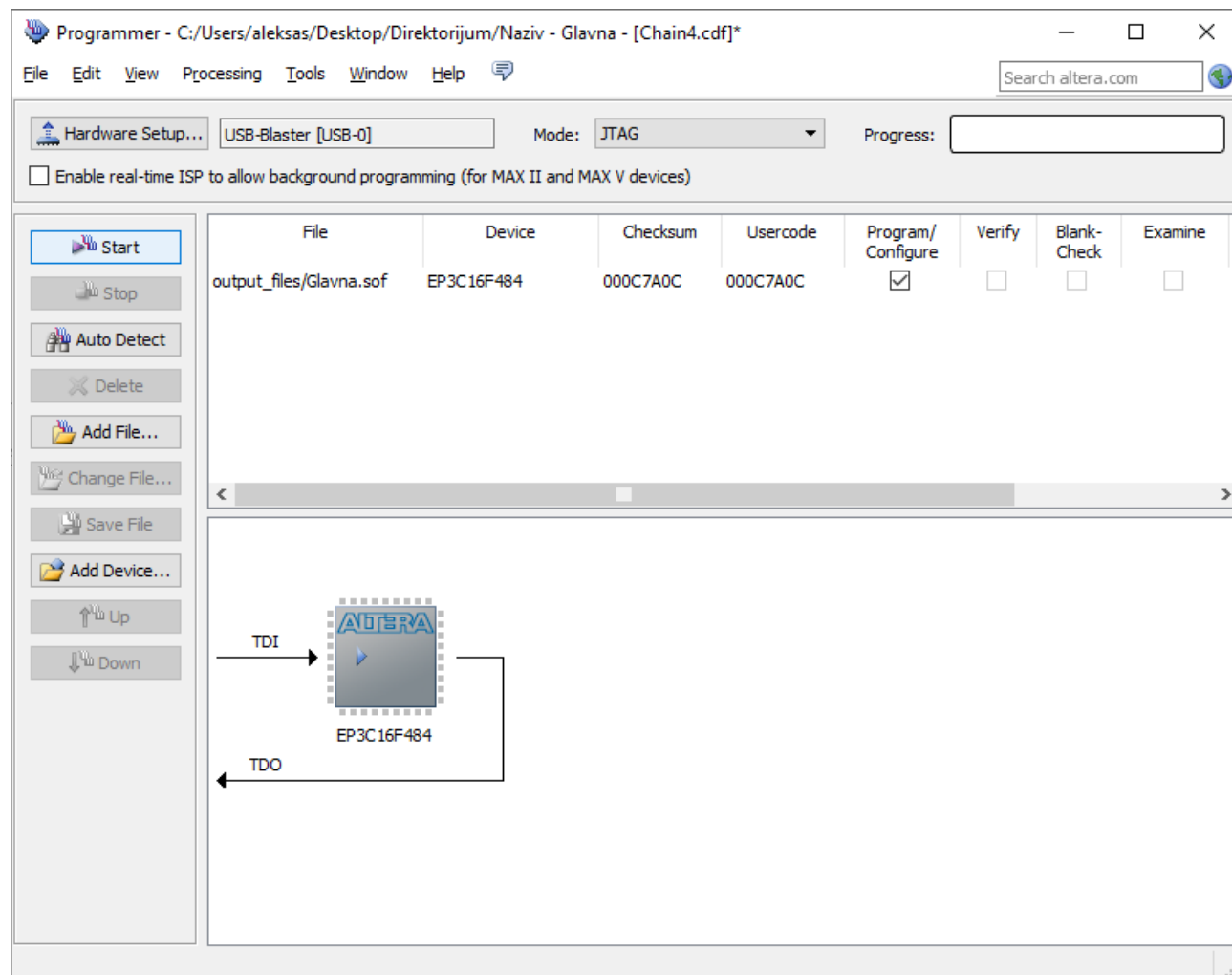
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- Hardware Setup...
- **Currently Selected Hardware -> Close**
- Start



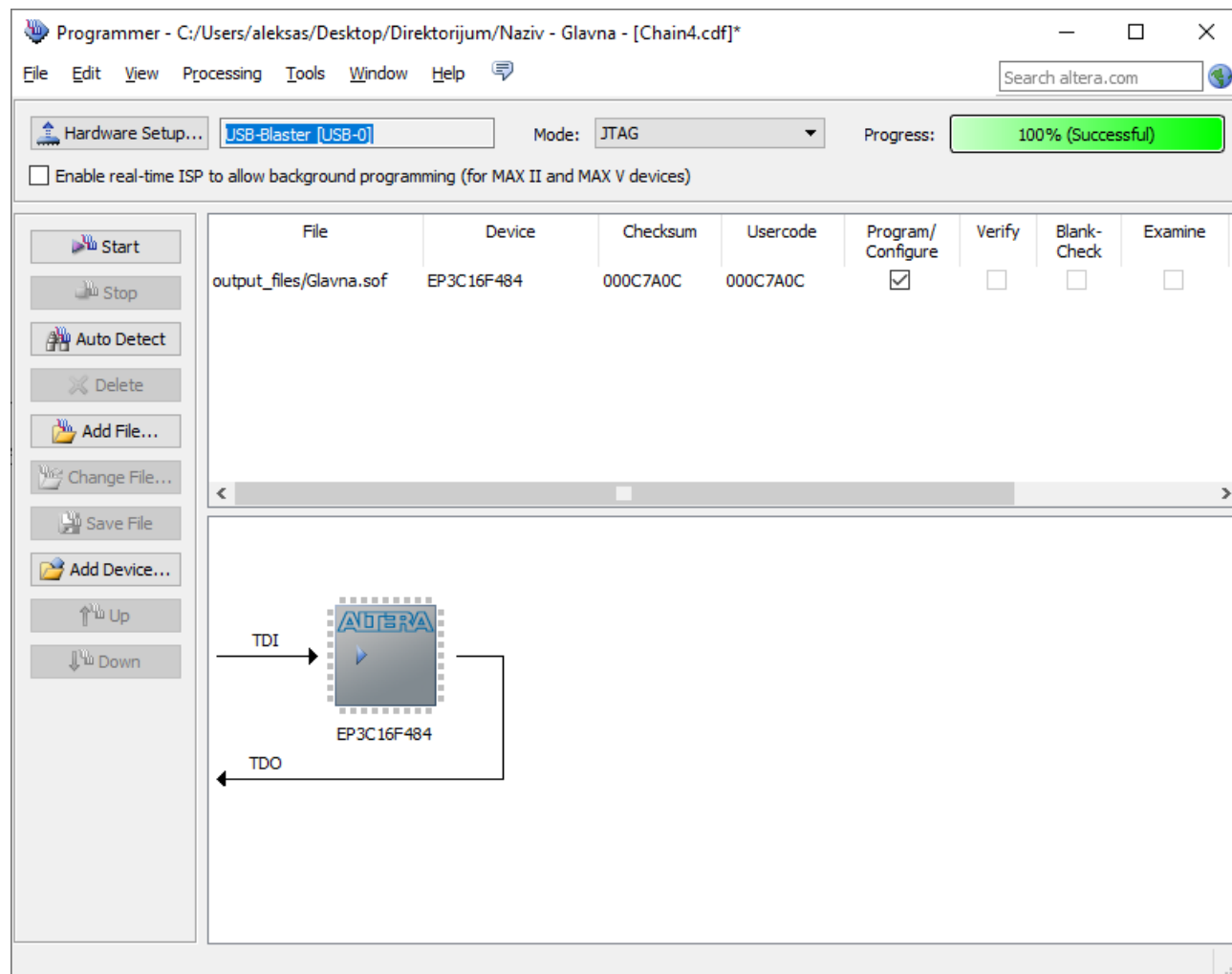
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- **Start**



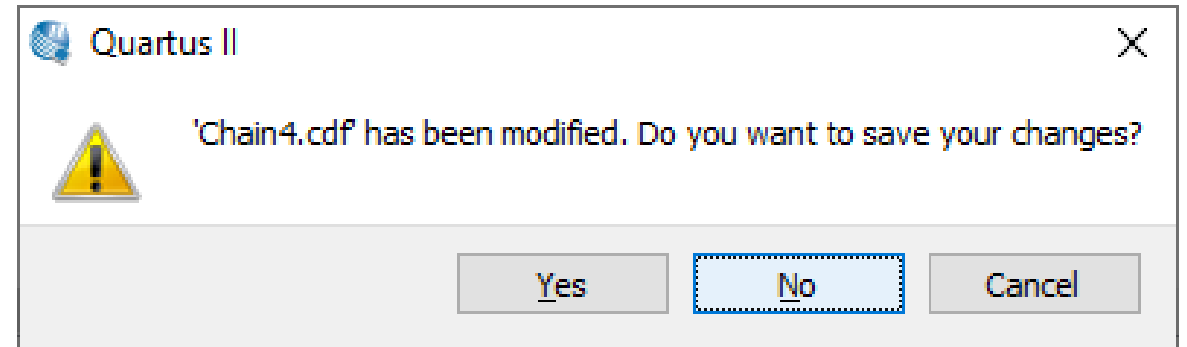
# Спуштање шеме на плочицу

- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- **Start**



# Спуштање шеме на плочицу

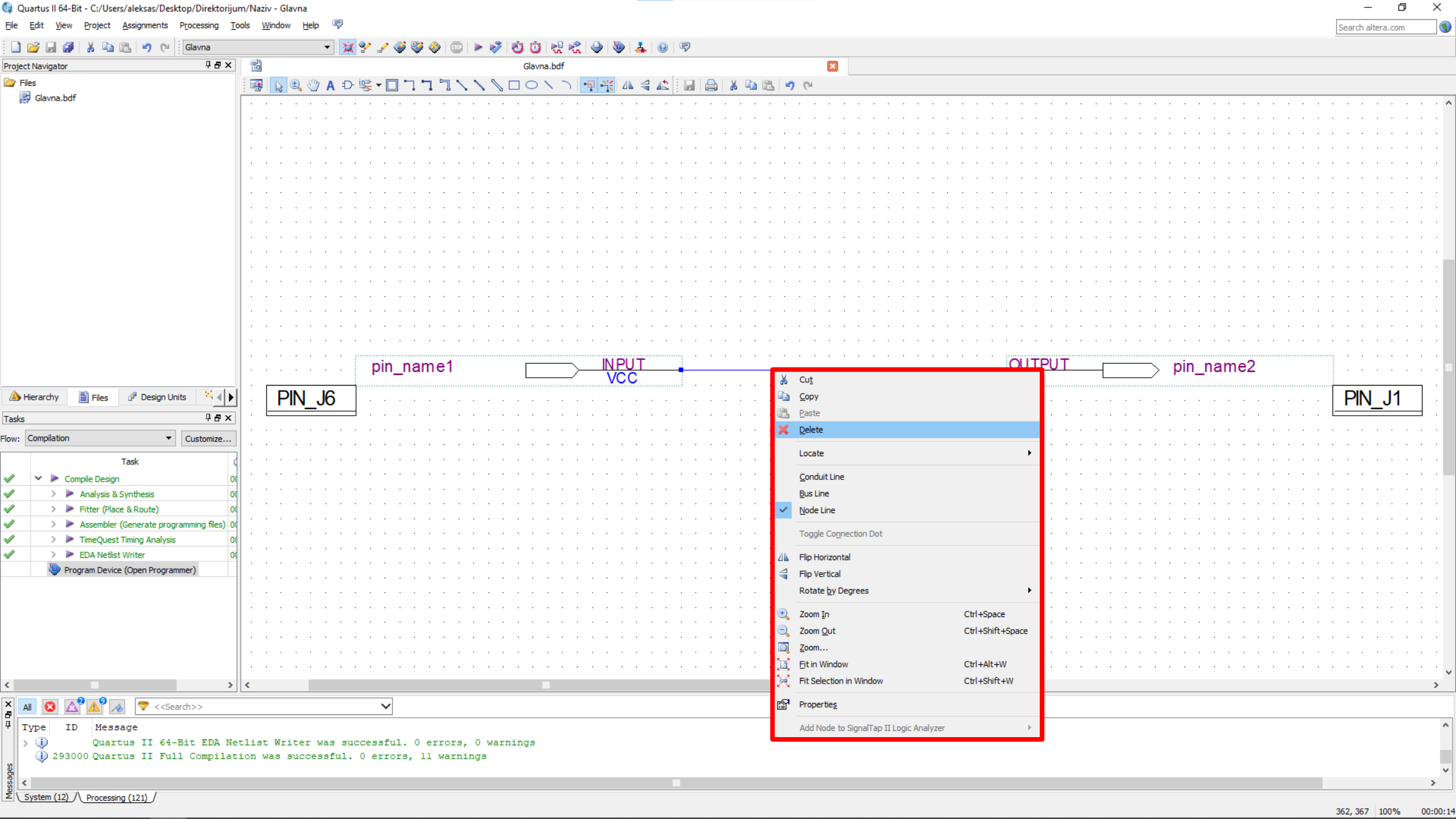
- Standard -> Start Compilation
- Standard -> Pin Planner
- Location -> Close
- Standard -> Start Compilation
- Tasks -> Program Device
- Add File...
- File Name -> Open
- Hardware Setup...
- Currently Selected Hardware -> Close
- **Start**



## Додавање симбола на шему

- Right Click -> Delete (Left Click -> Del)
- Block Editor -> Symbol Tool (Double Left Click)
- Name -> Repeat-insert mode -> OK
- Left Click -> Esc
- Block Editor -> Orthogonal Node Tool -> Left Click & Drag -> Left Click & Drag -> Esc





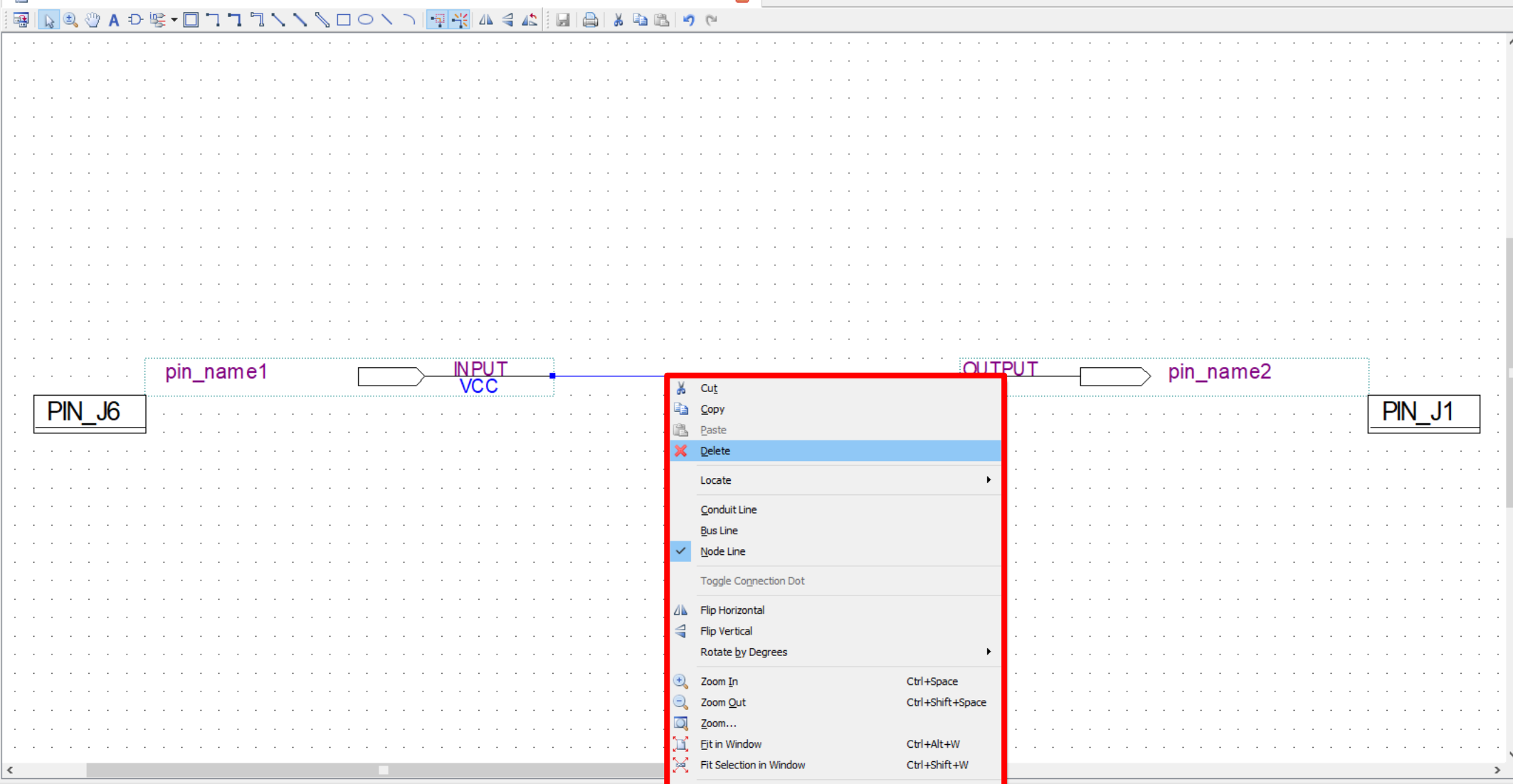
Files  
Glavna.bdf

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Progress
Compile Design	00%
Analysis & Synthesis	00%
Fitter (Place & Route)	00%
Assembler (Generate programming files)	00%
TimeQuest Timing Analysis	00%
EDA Netlist Writer	00%
Program Device (Open Programmer)	

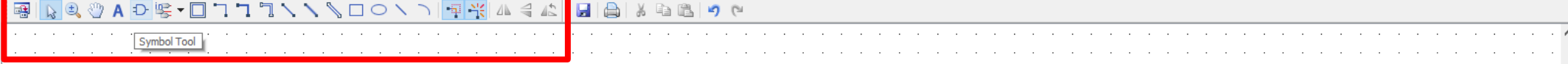
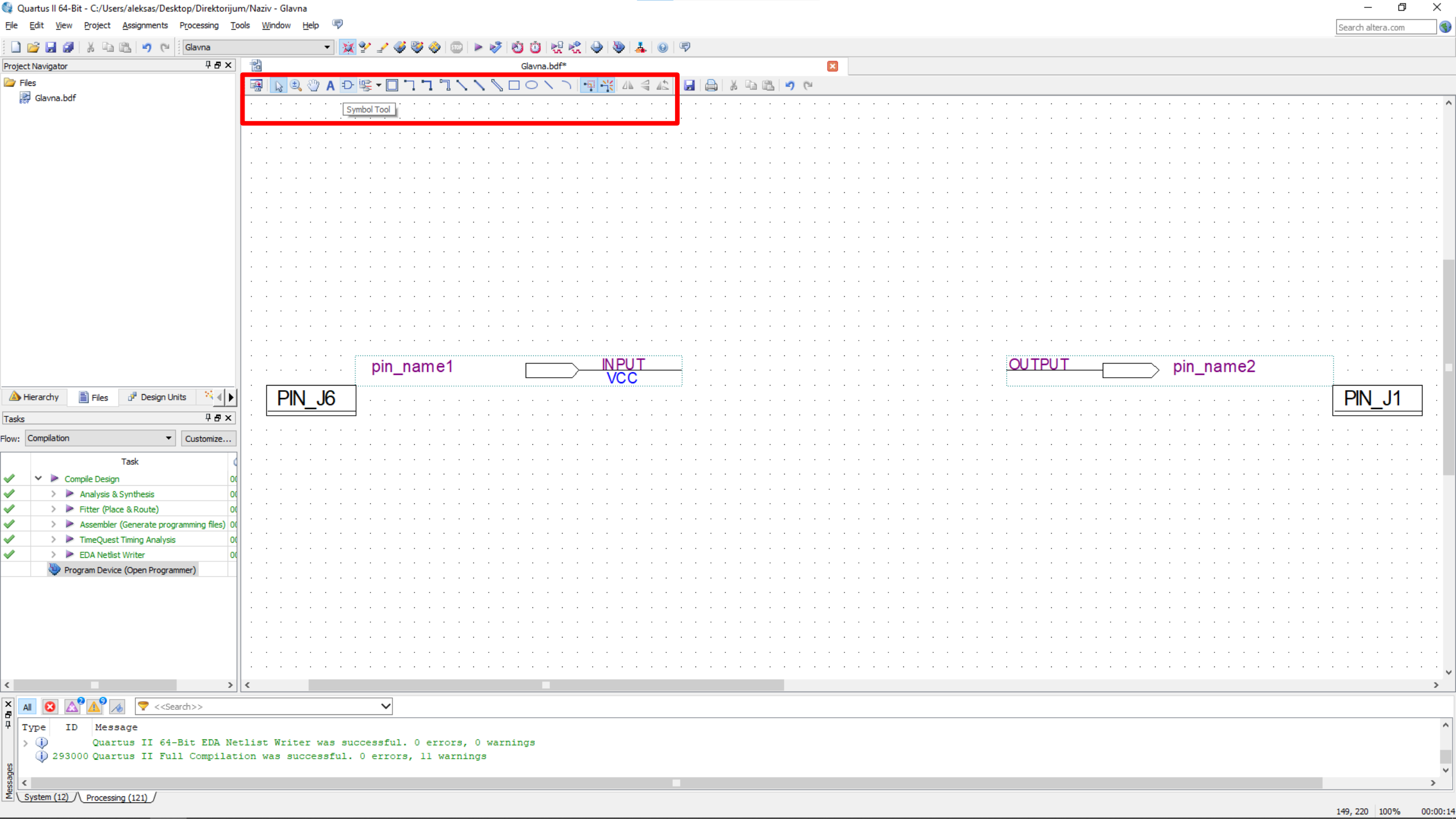


- Cut
- Copy
- Paste
- Delete
- Locate
- Conduit Line
- Bus Line
- Node Line
- Toggle Connection Dot
- Flip Horizontal
- Flip Vertical
- Rotate by Degrees
- Zoom In Ctrl+Space
- Zoom Out Ctrl+Shift+Space
- Zoom...
- Fit in Window Ctrl+Alt+W
- Fit Selection in Window Ctrl+Shift+W
- Properties
- Add Node to SignalTap II Logic Analyzer

All <<Search>>

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>		293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

System (12) / Processing (121)



Flow: Compilation

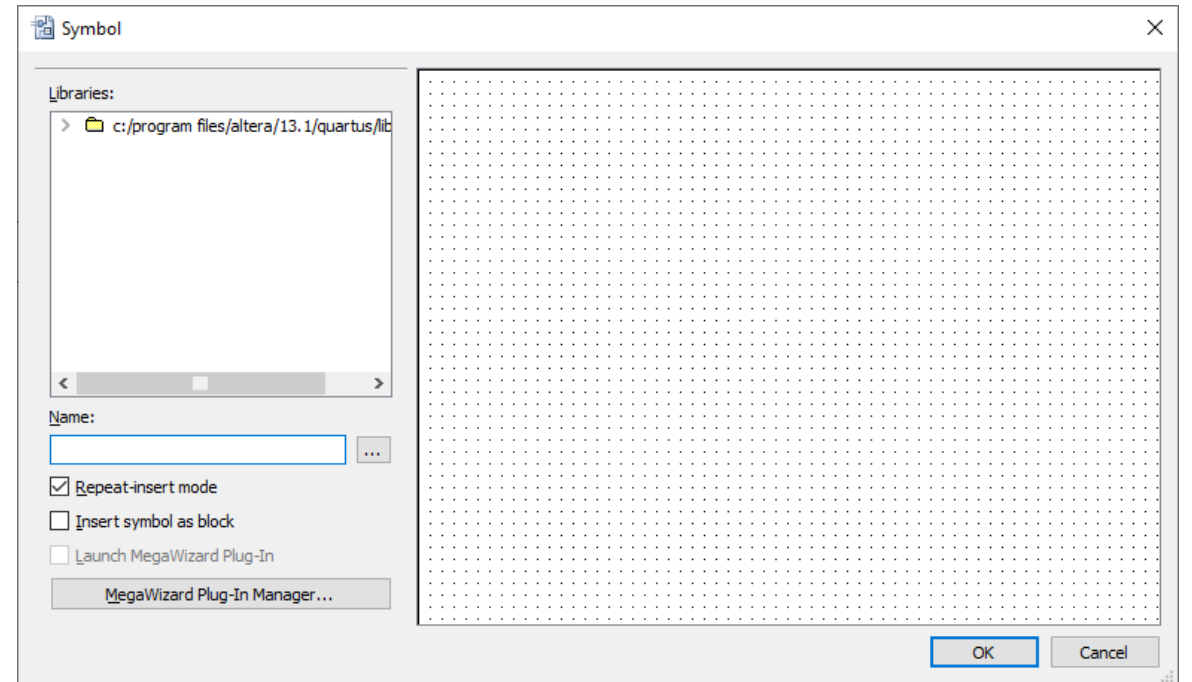
Task	Progress
Compile Design	00%
> Analysis & Synthesis	00%
> Fitter (Place & Route)	00%
> Assembler (Generate programming files)	00%
> TimeQuest Timing Analysis	00%
> EDA Netlist Writer	00%
Program Device (Open Programmer)	



Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 11 warnings

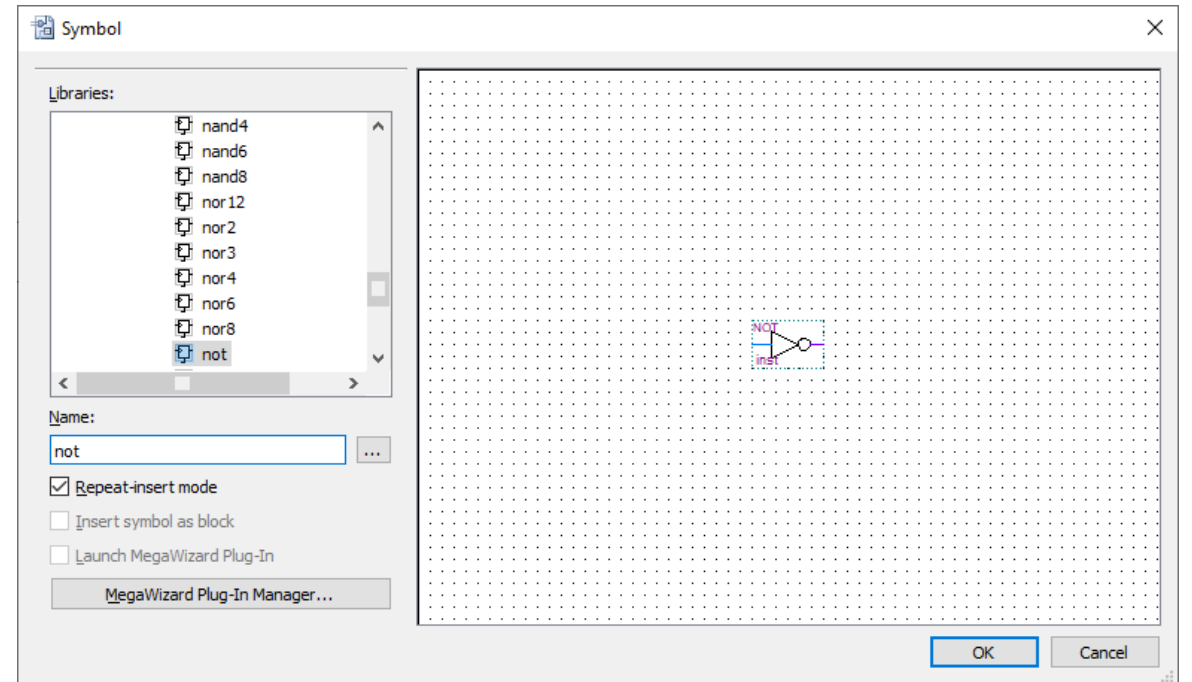
# Додавање симбола на шему

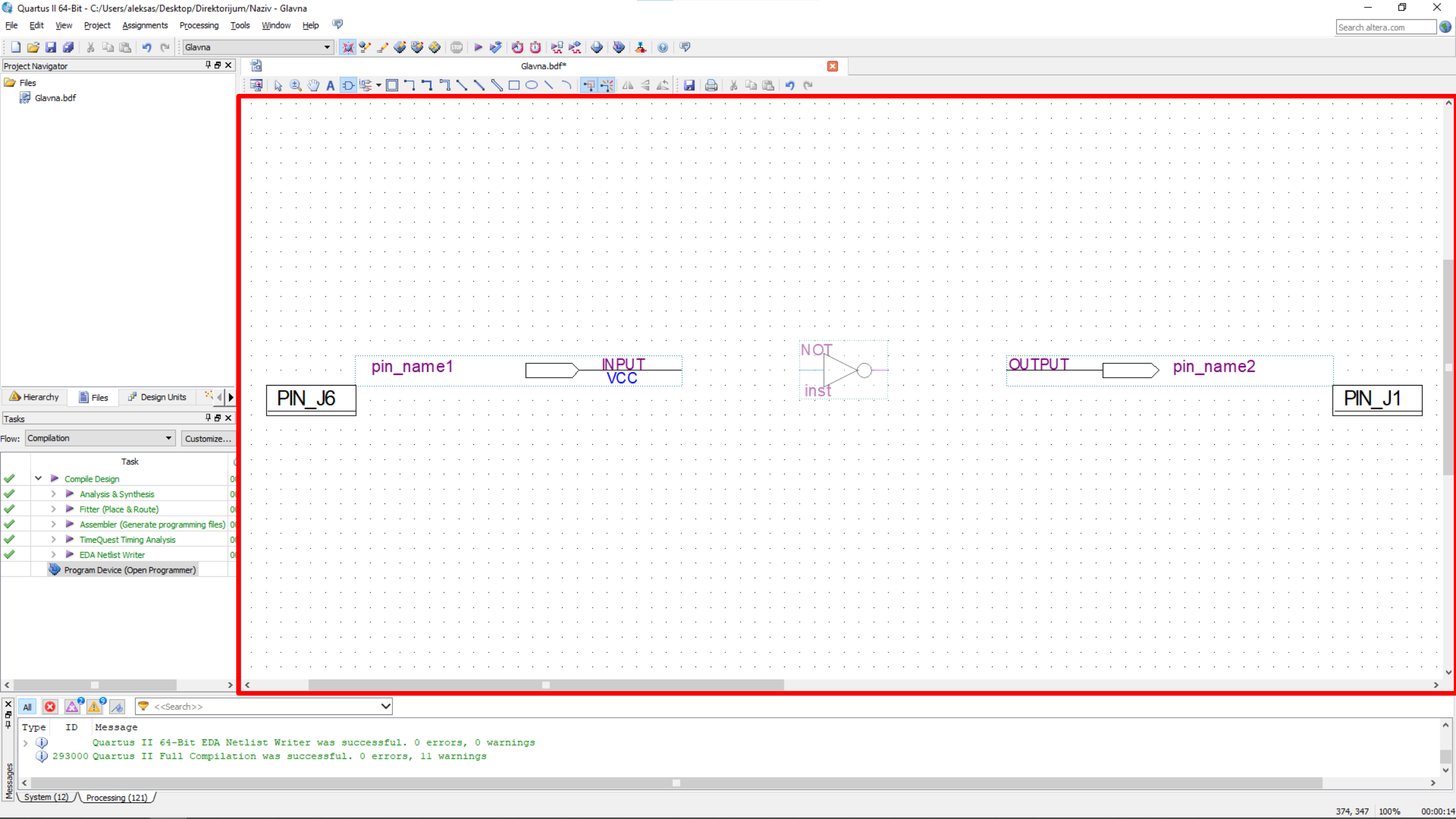
- Right Click -> Delete (Left Click -> Del)
- Block Editor -> Symbol Tool (Double Left Click)
- **Name -> Repeat-insert mode -> OK**
- Left Click -> Esc
- Block Editor -> Orthogonal Node Tool -> Left Click & Drag -> Left Click & Drag -> Esc

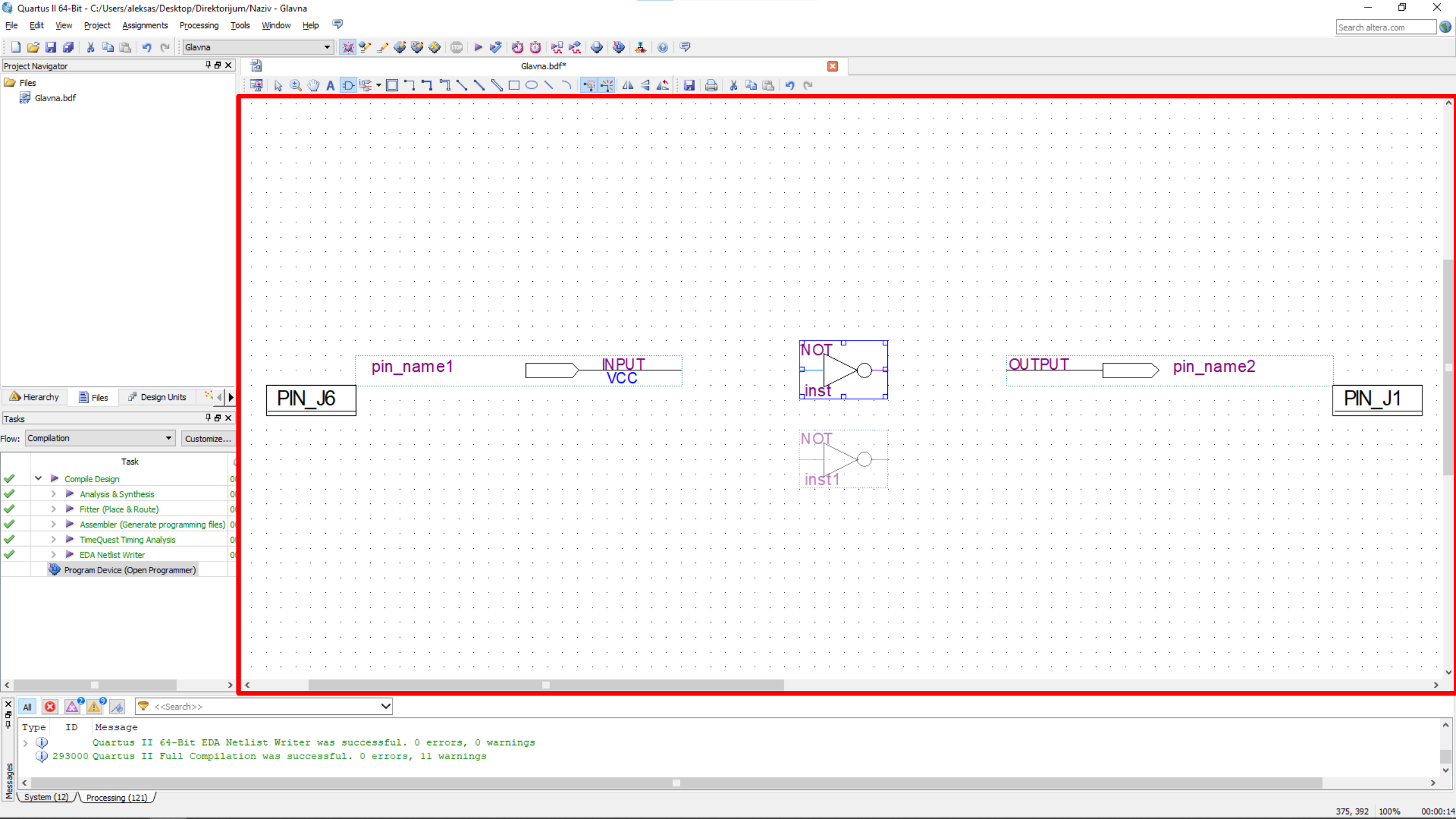


# Додавање симбола на шему

- Right Click -> Delete (Left Click -> Del)
- Block Editor -> Symbol Tool (Double Left Click)
- **Name -> Repeat-insert mode -> OK**
- Left Click -> Esc
- Block Editor -> Orthogonal Node Tool -> Left Click & Drag -> Left Click & Drag -> Esc







Files

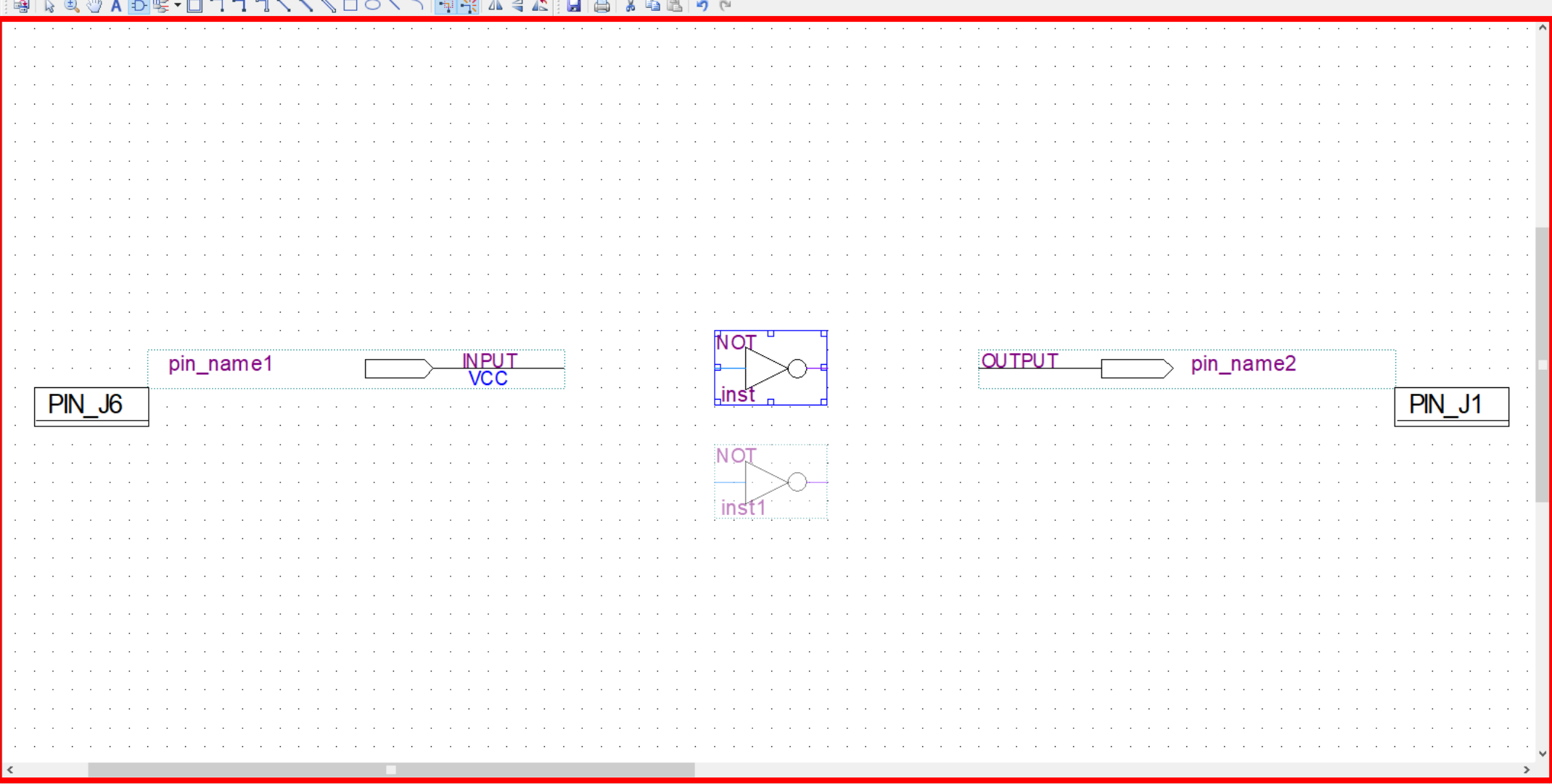
- Glavna.bdf

Hierarchy | Files | Design Units

Tasks

Flow: Compilation

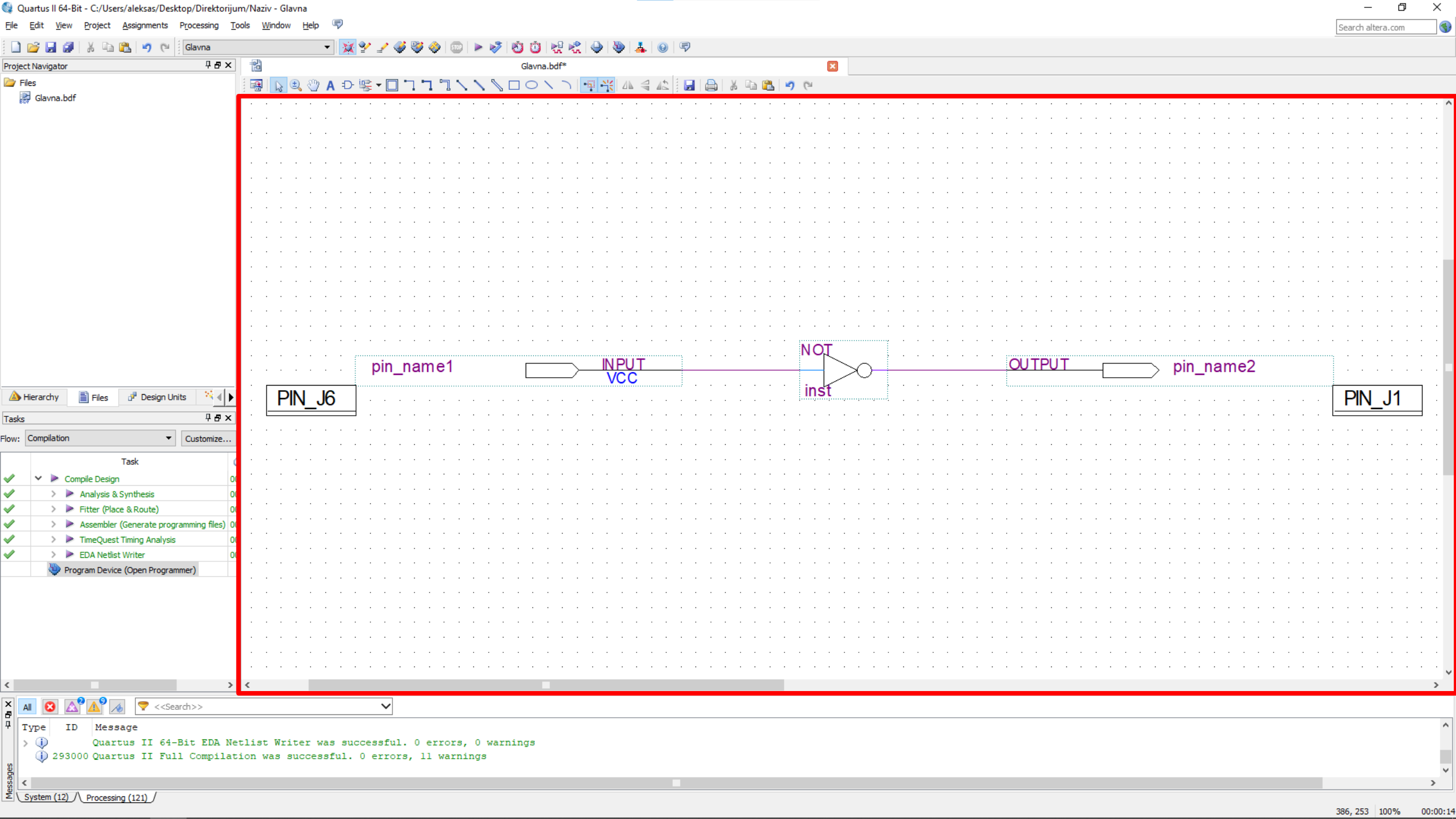
Task	Progress
Compile Design	0%
> Analysis & Synthesis	0%
> Fitter (Place & Route)	0%
> Assembler (Generate programming files)	0%
> TimeQuest Timing Analysis	0%
> EDA Netlist Writer	0%
Program Device (Open Programmer)	



Messages

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 11 warnings

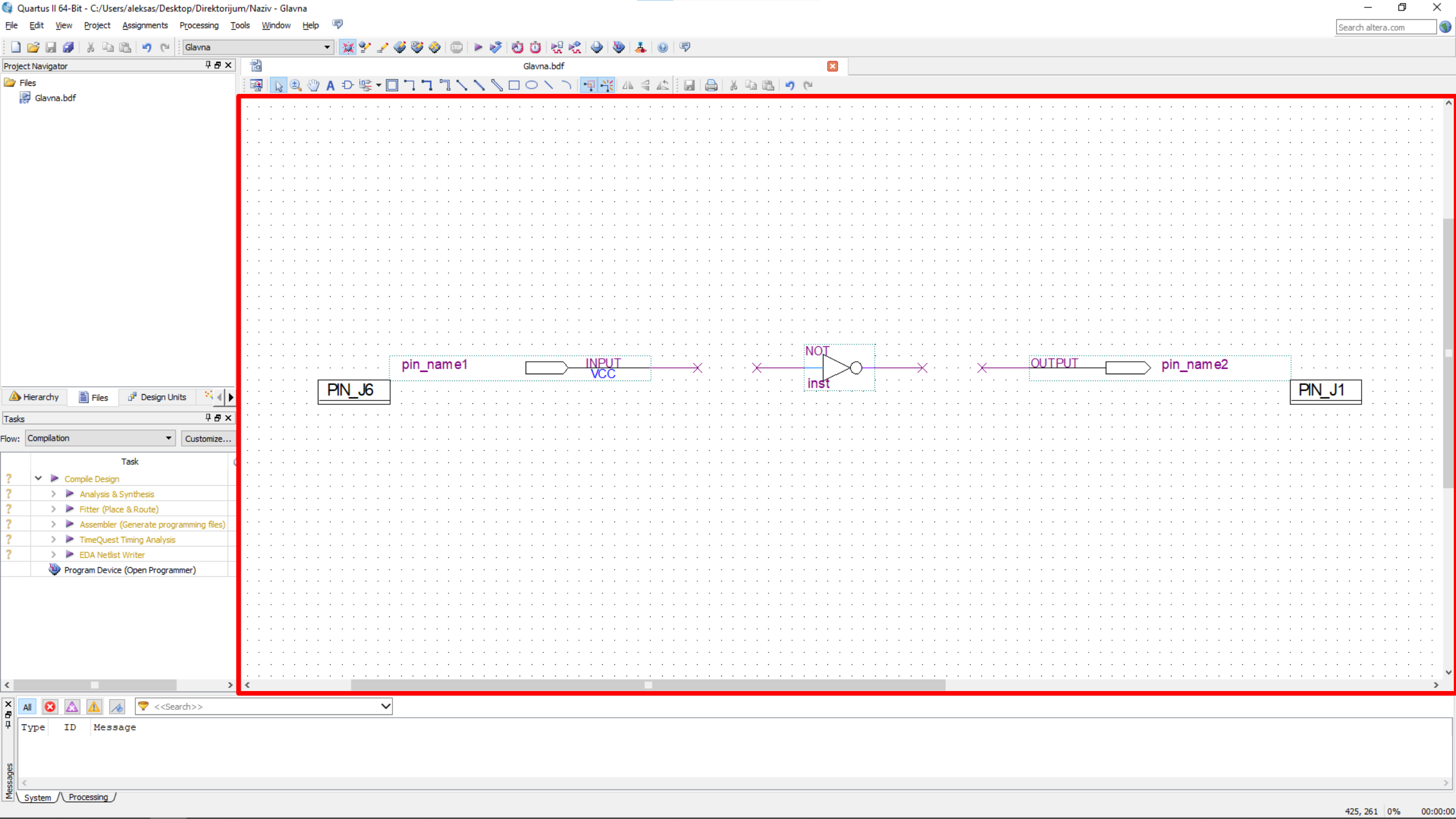
System (12) / Processing (121)



# Именовање сигнала

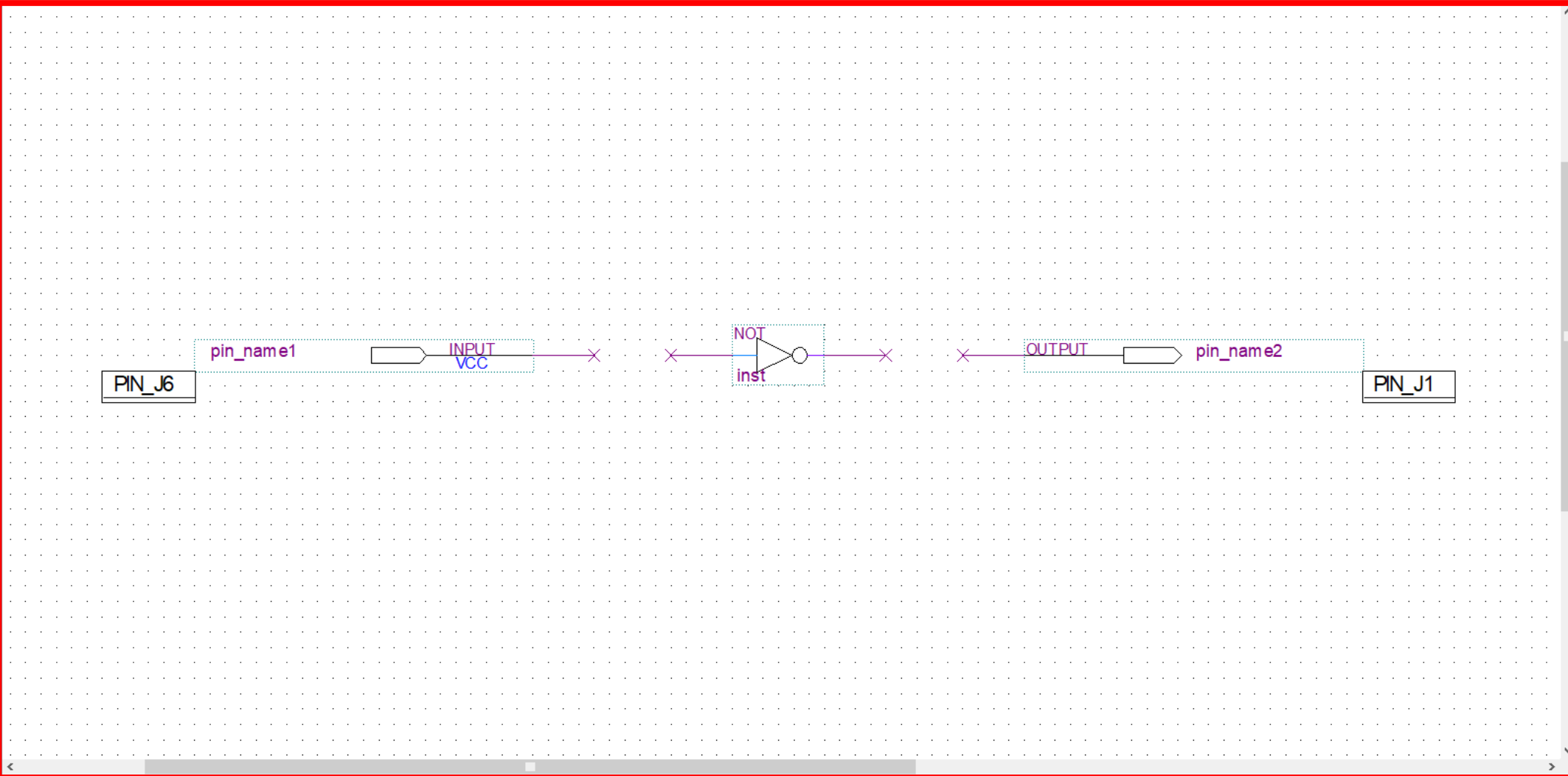
- Right Click -> Properties (Double Left Click)
- Pin name(s) -> OK
- Right Click -> Properties (Left Click & Type)
- Name -> OK
- Pin Planner
- Node Name -> Del
- Yes
- Location -> Close





Project Navigator  
Files  
Glavna.bdf

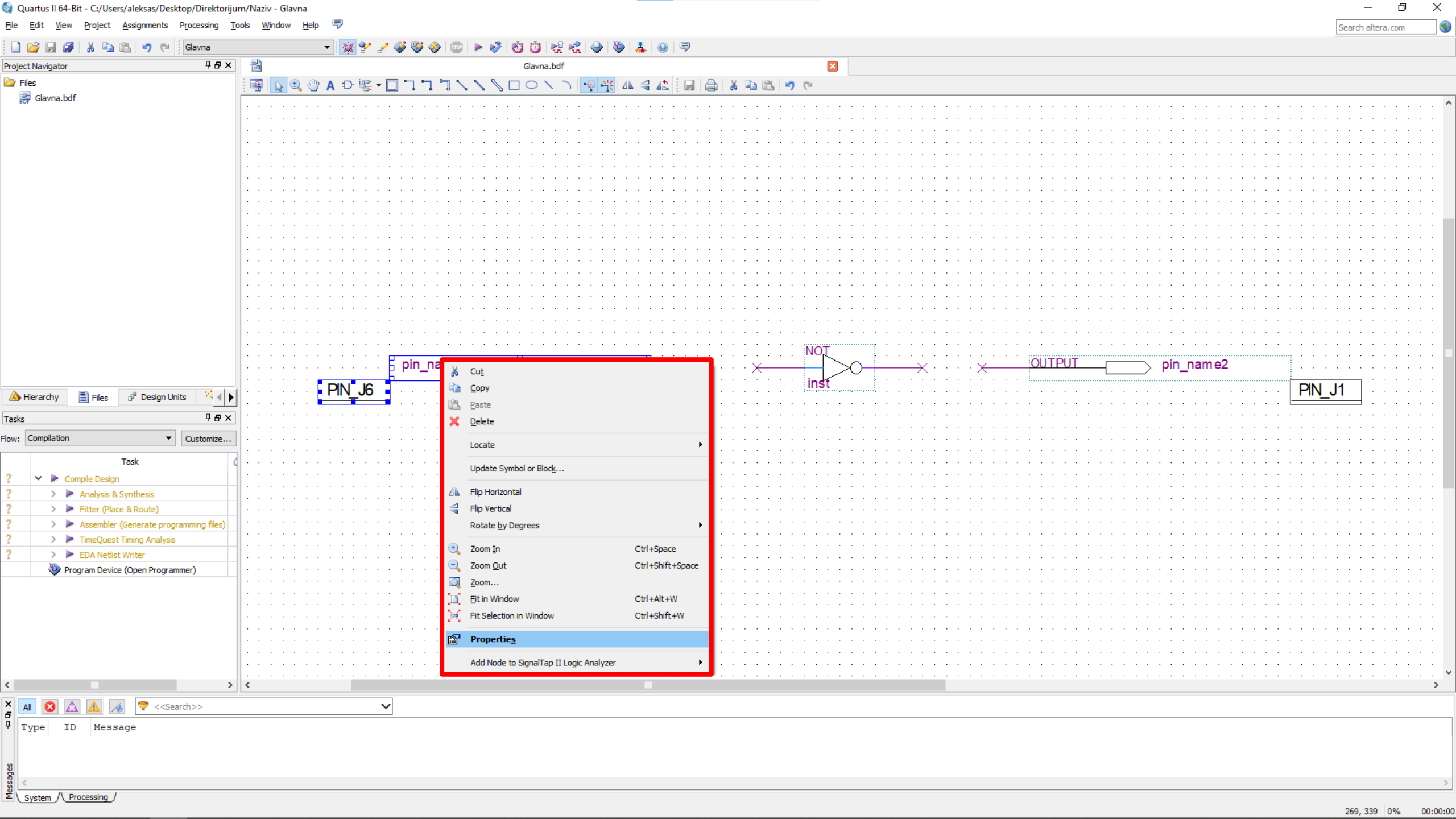
Glavna.bdf



Hierarchy Files Design Units  
Tasks  
Flow: Compilation  
Task  
Compile Design  
Analysis & Synthesis  
Fitter (Place & Route)  
Assembler (Generate programming files)  
TimeQuest Timing Analysis  
EDA Netlist Writer  
Program Device (Open Programmer)

All <<Search>>

Messages  
Type ID Message  
System Processing



Project Navigator

Files

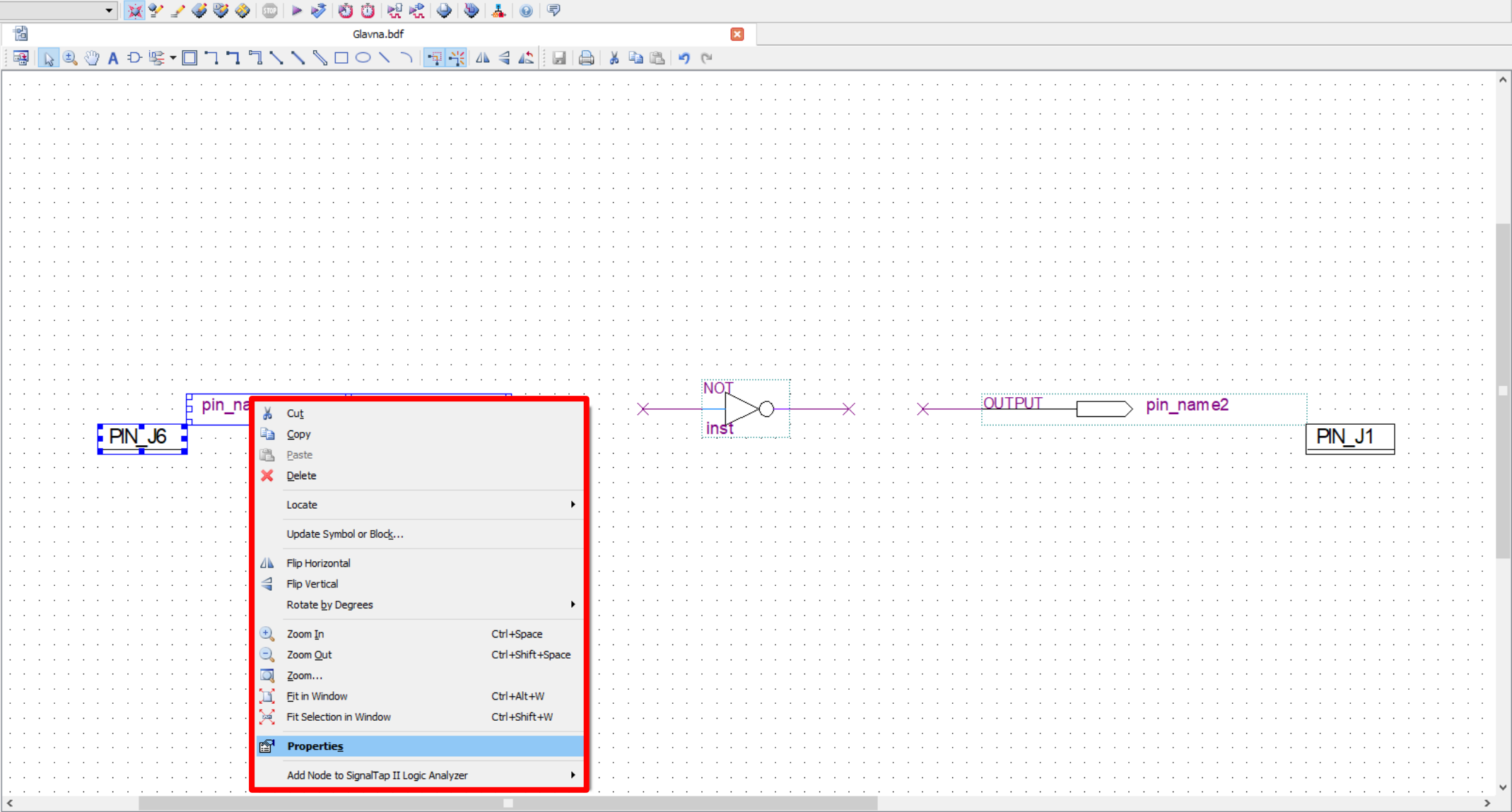
- Glavna.bdf

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)



Messages

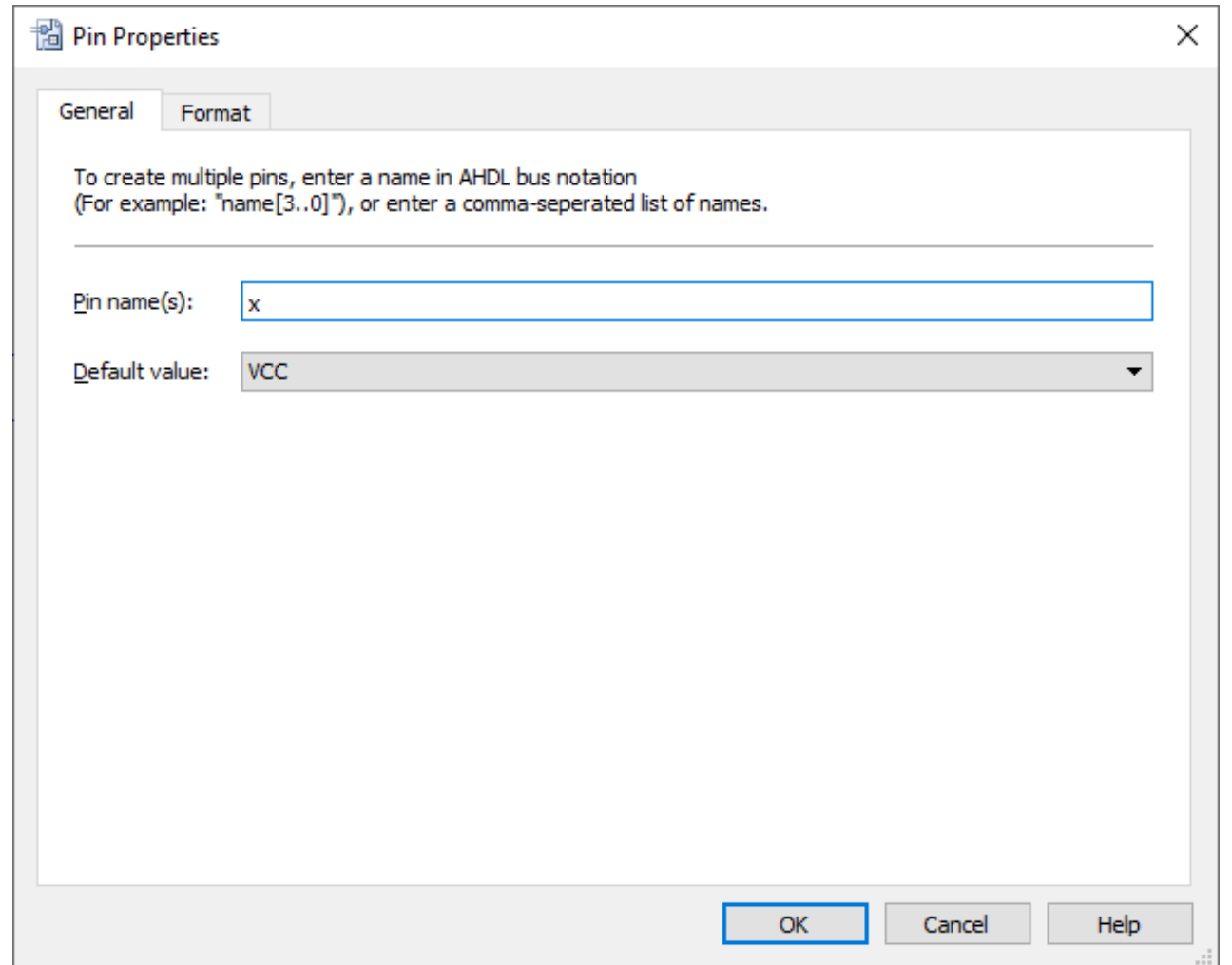
Type	ID	Message
------	----	---------

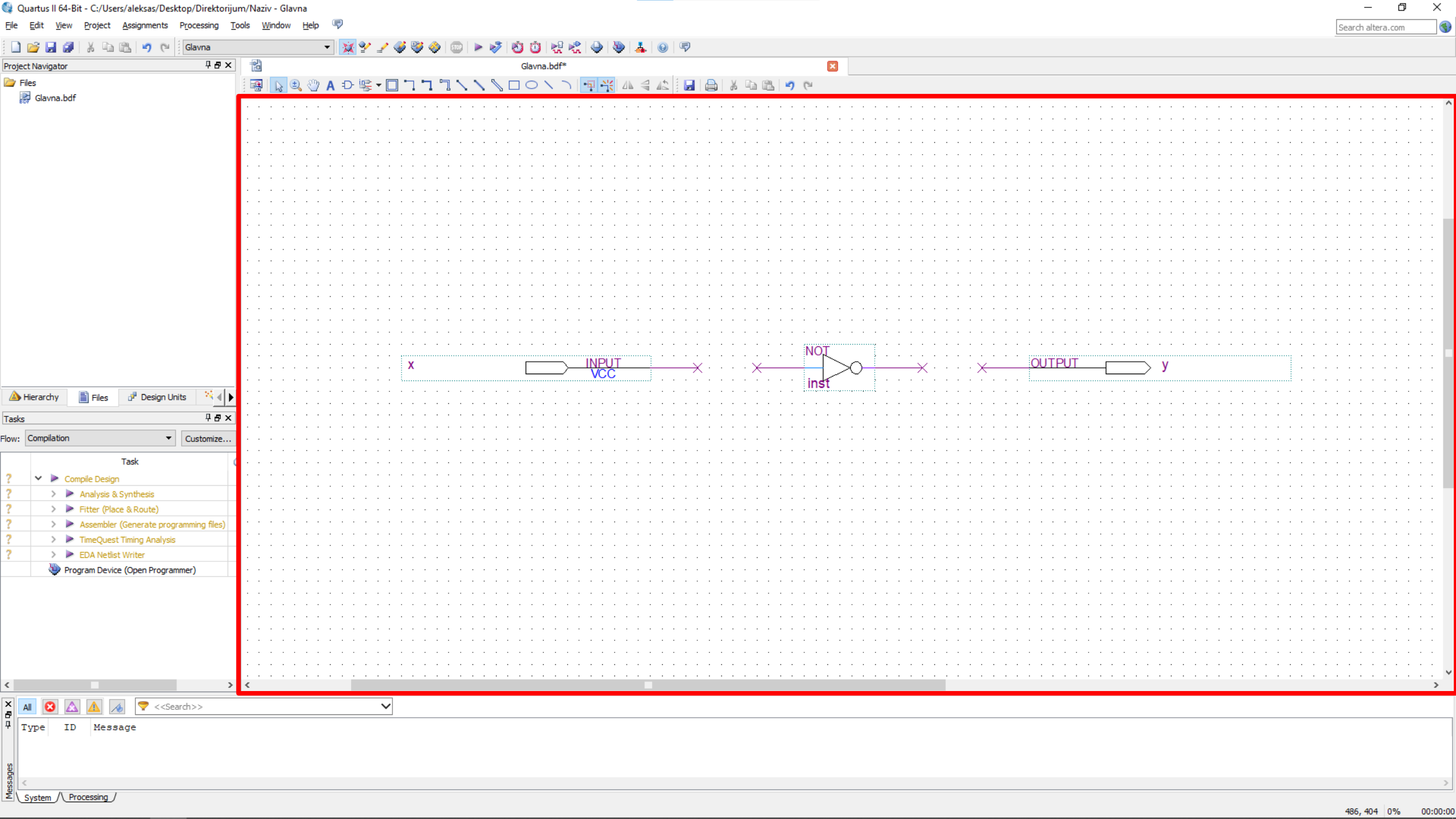
System / Processing

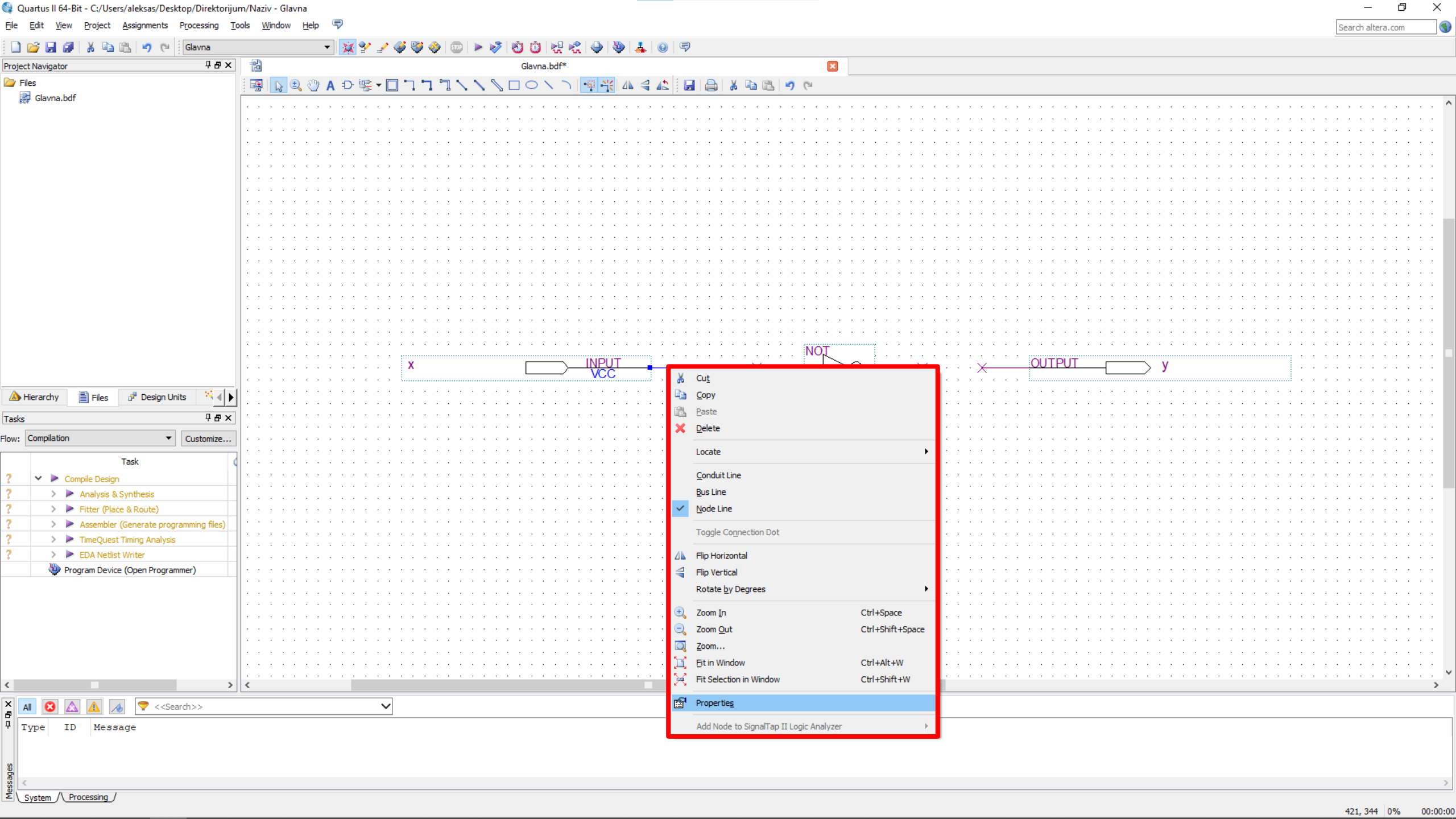
269,339 0% 00:00:00

# Именовање сигнала

- Right Click -> Properties (Double Left Click)
- **Pin name(s) -> OK**
- Right Click -> Properties (Left Click & Type)
- Name -> OK
- Pin Planner
- Node Name -> Del
- Yes
- Location -> Close





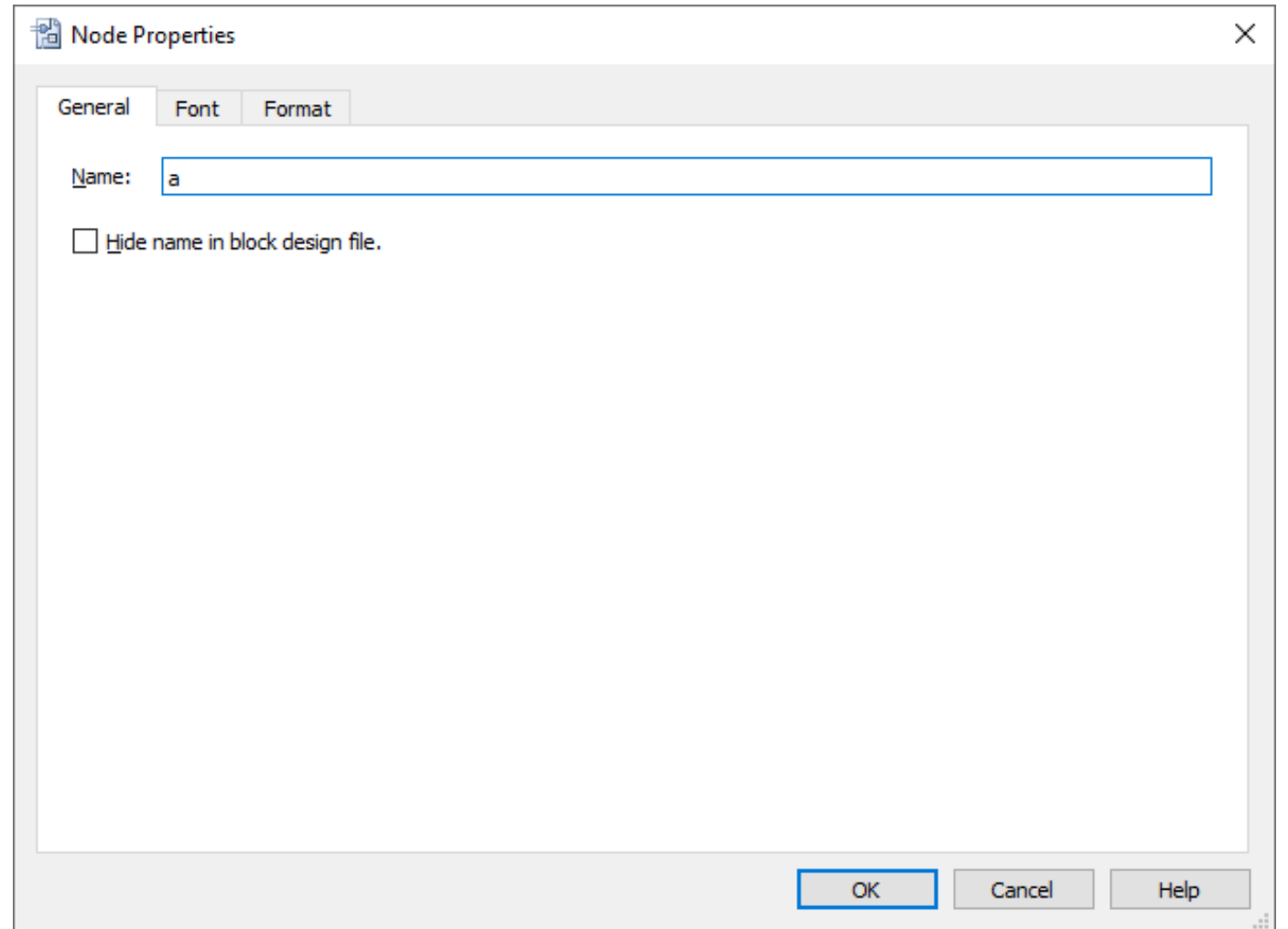


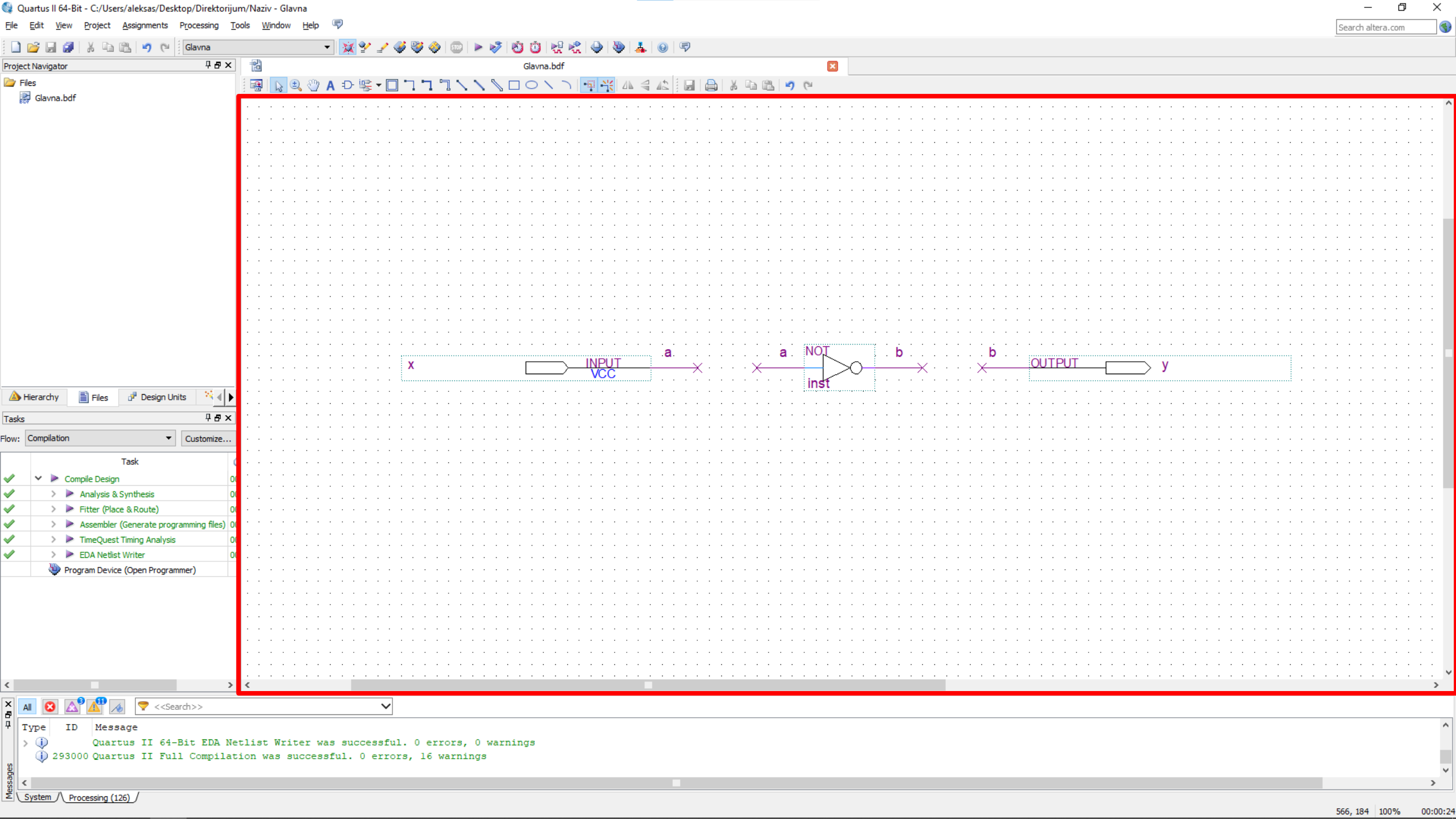
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Type	ID	Message
System	Processing	

# Именовање сигнала

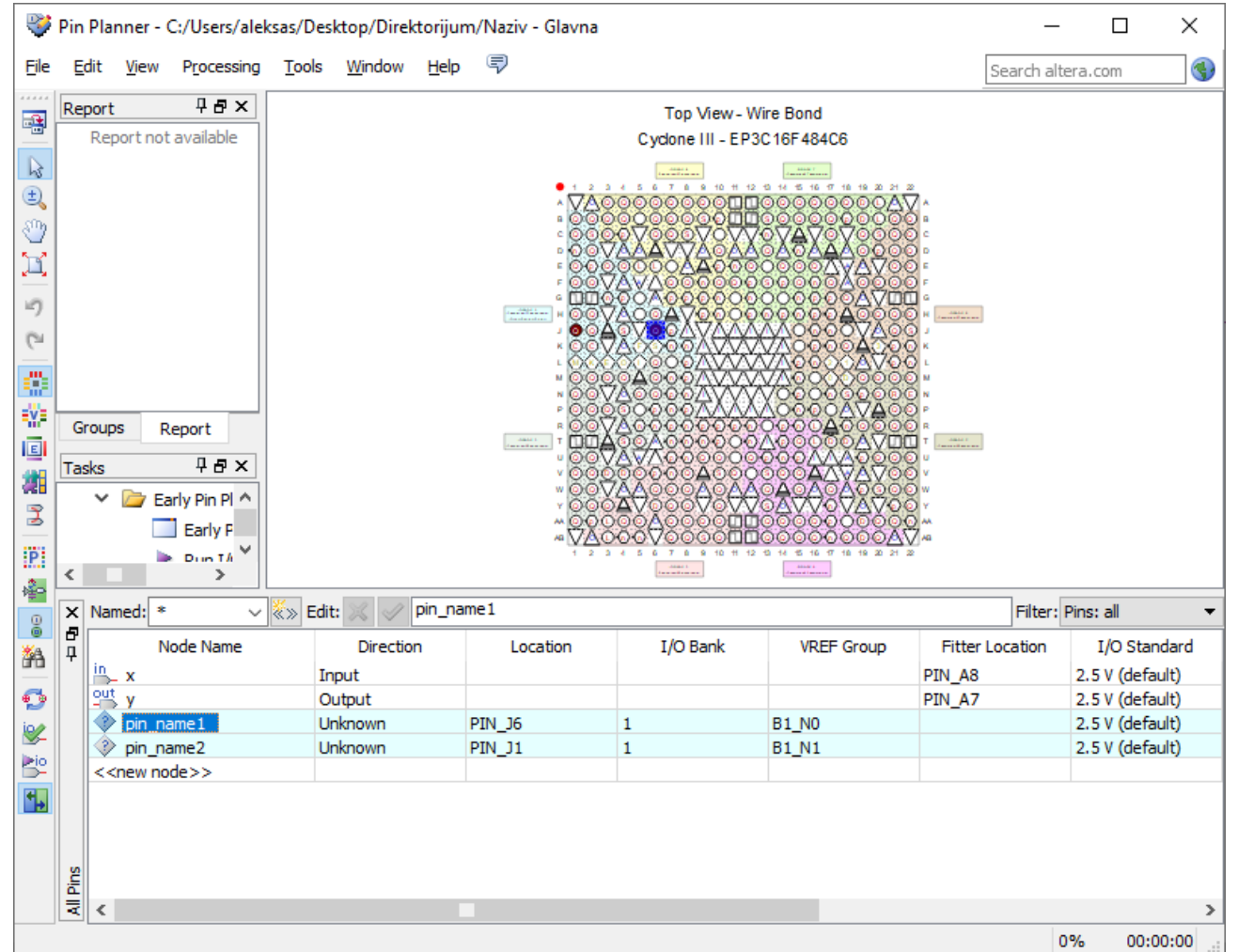
- Right Click -> Properties (Double Left Click)
- Pin name(s) -> OK
- Right Click -> Properties (Left Click & Type)
- **Name -> OK**
- Pin Planner
- Node Name -> Del
- Yes
- Location -> Close





# Именовање сигнала

- Right Click -> Properties (Double Left Click)
- Pin name(s) -> OK
- Right Click -> Properties (Left Click & Type)
- Name -> OK
- Pin Planner
- **Node Name -> Del**
- Yes
- Location -> Close



Pin Planner - C:/Users/aleksas/Desktop/Direktorijum/Naziv - Glavna

File Edit View Processing Tools Window Help

Search altera.com

Report Report not available

Groups Report

Tasks Early Pin Pl Early P Pin TA

Named: \* Edit: pin\_name1 Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in_x	Input				PIN_A8	2.5 V (default)
out_y	Output				PIN_A7	2.5 V (default)
pin_name1	Unknown	PIN_J6	1	B1_N0		2.5 V (default)
pin_name2	Unknown	PIN_J1	1	B1_N1		2.5 V (default)
<<new node>>						

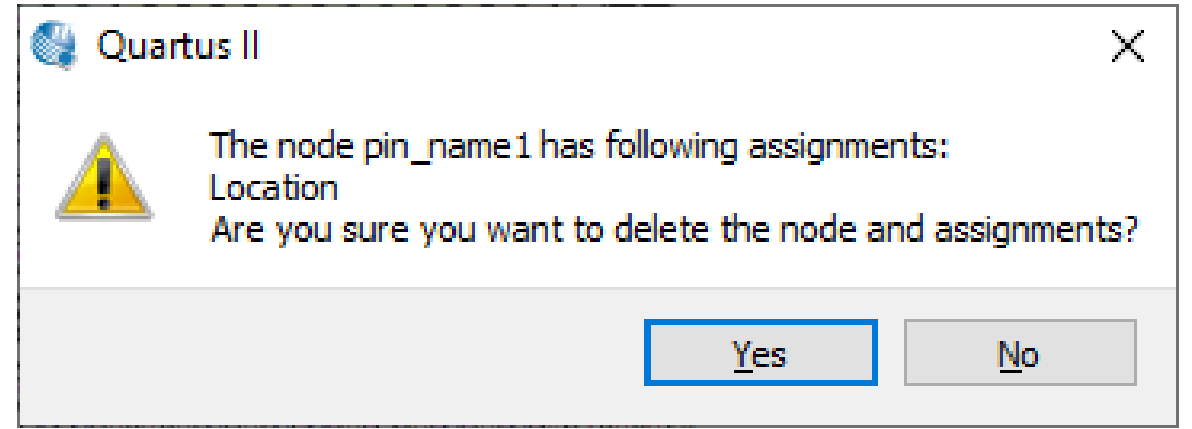
All Pins

0% 00:00:00



# Именовање сигнала

- Right Click -> Properties (Double Left Click)
- Pin name(s) -> OK
- Right Click -> Properties (Left Click & Type)
- Name -> OK
- Pin Planner
- Node Name -> Del
- **Yes**
- Location -> Close



# Именовање сигнала

- Right Click -> Properties (Double Left Click)
- Pin name(s) -> OK
- Right Click -> Properties (Left Click & Type)
- Name -> OK
- Pin Planner
- Node Name -> Del
- Yes
- **Location -> Close**

Pin Planner - C:/Users/aleksas/Desktop/Direktorijum/Naziv - Glavna

File Edit View Processing Tools Window Help

Search altera.com

Report Report not available

Groups Report

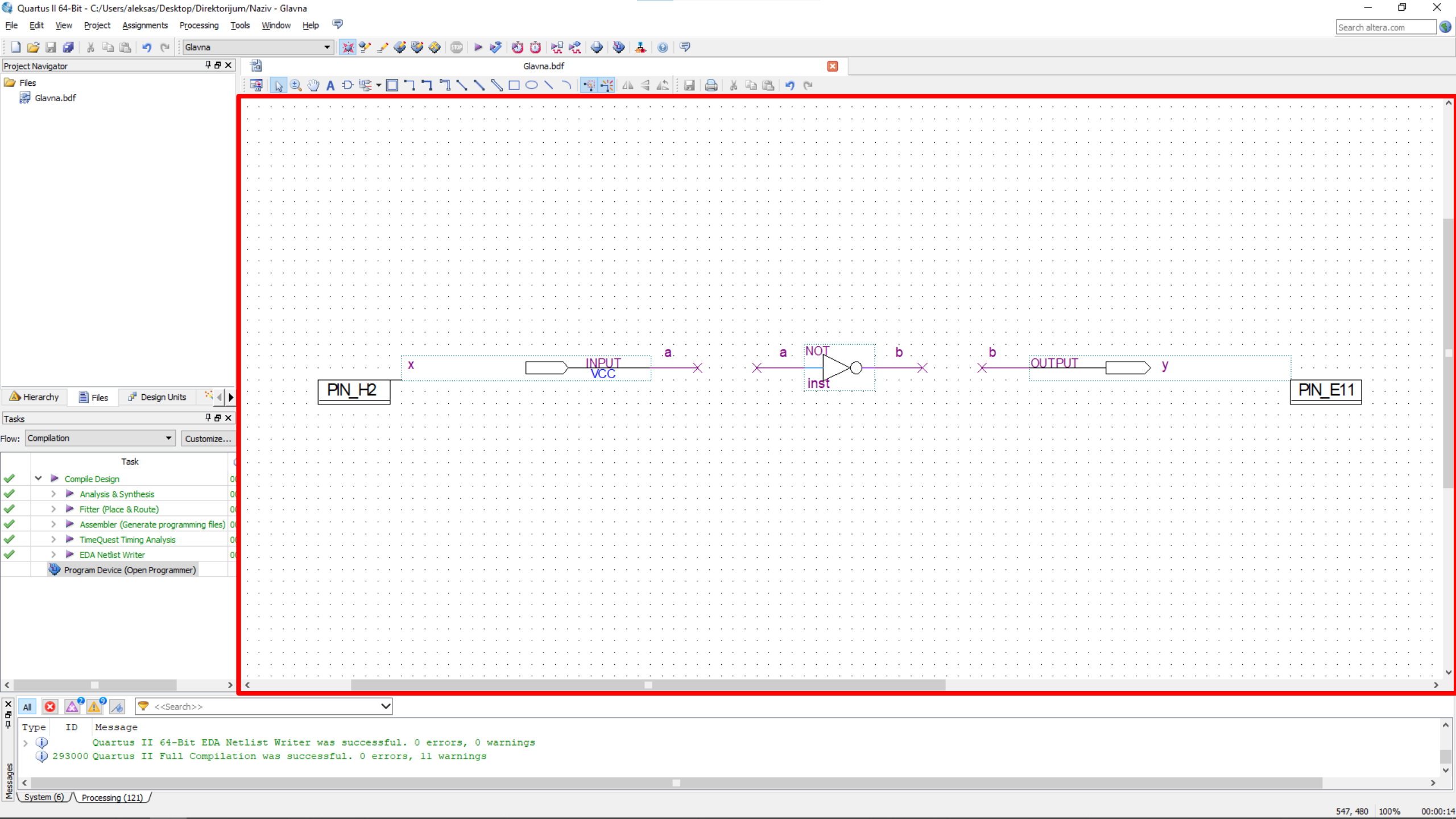
Tasks Early Pin Pl Early P Pin TA

Named: \* Edit: Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in x	Input	PIN_H2	1	B1_N1	PIN_A8	2.5 V (default)
out y	Output	PIN_E11	7	B7_N1	PIN_A7	2.5 V (default)
<<new node>>						

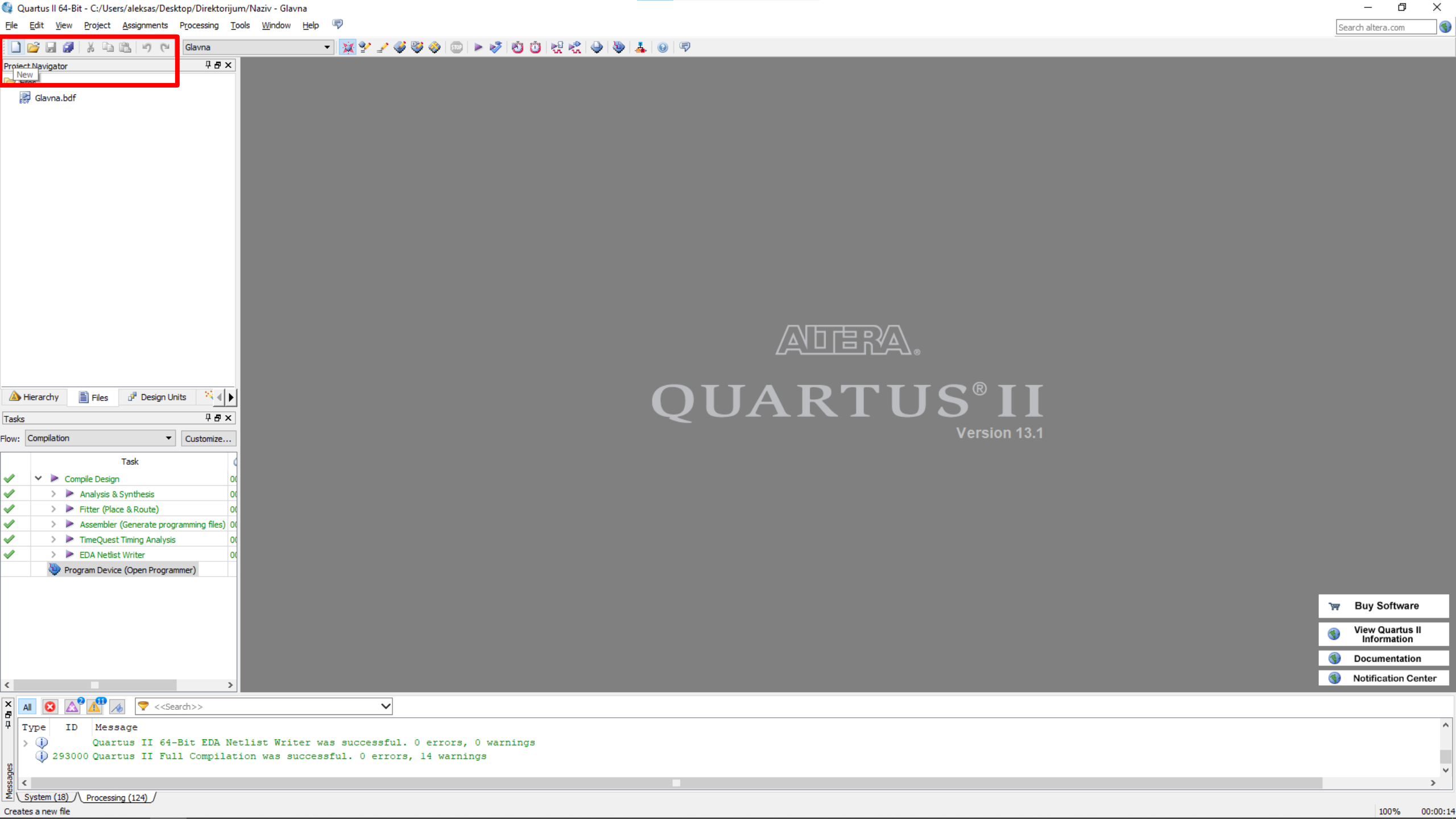
All Pins

0% 00:00:00



# Додавање помоћне шеме

- File -> New
- Design Files -> Block Diagram/Schematic File -> OK
- File -> Save As...
- File Name -> Add file to current project -> Save
- Standard -> Start Compilation



ALTEA

QUARTUS II

Version 13.1

Project Navigator

- New
- Glavna.bdf

Hierarchy | Files | Design Units

Tasks

Flow: Compilation | Customize...

Task	Progress
Compile Design	00
> Analysis & Synthesis	00
> Fitter (Place & Route)	00
> Assembler (Generate programming files)	00
> TimeQuest Timing Analysis	00
> EDA Netlist Writer	00
Program Device (Open Programmer)	

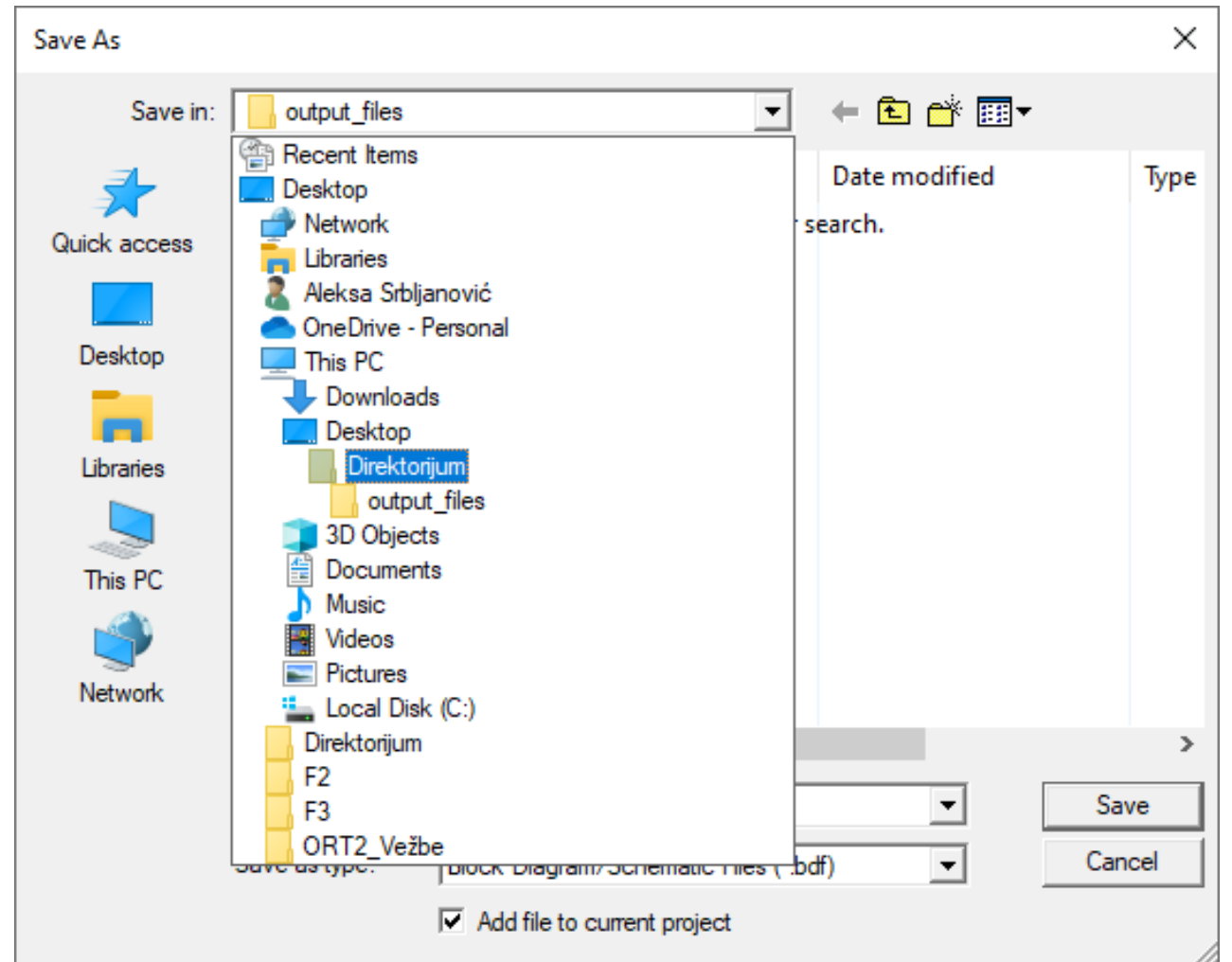
- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

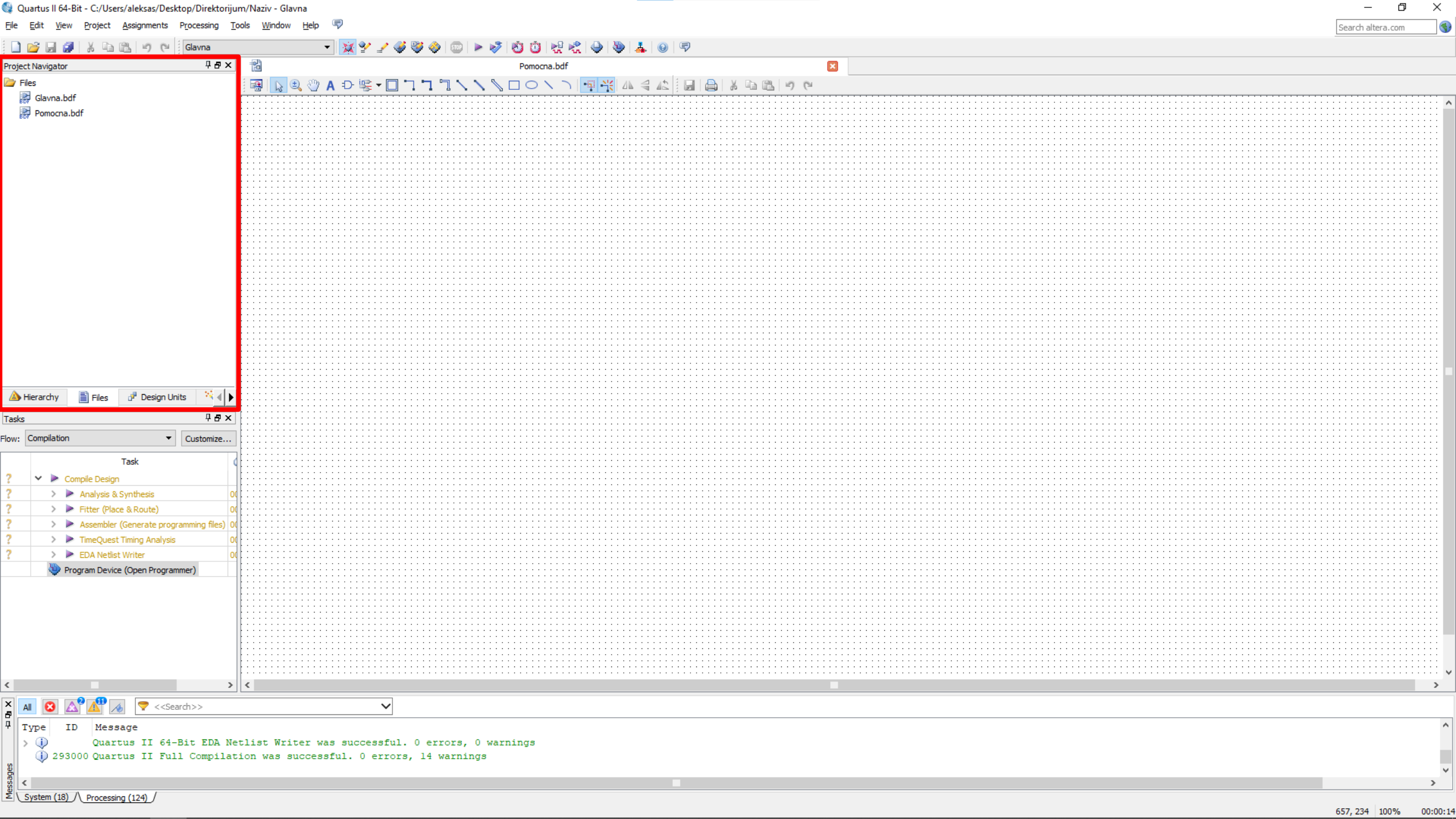
All | <<Search>>

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 14 warnings

# Додавање помоћне шеме

- File -> New
- Design Files -> Block Diagram/Schematic File -> OK
- File -> Save As...
- **File Name -> Add file to current project -> Save**
- Standard -> Start Compilation





**Project Navigator**

Files

- Glavna.bdf
- Pomocna.bdf

Hierarchy | Files | Design Units

**Pomocna.bdf**

Blank schematic editor area with a grid background.

**Tasks**

Flow: **Compilation** | Customize...

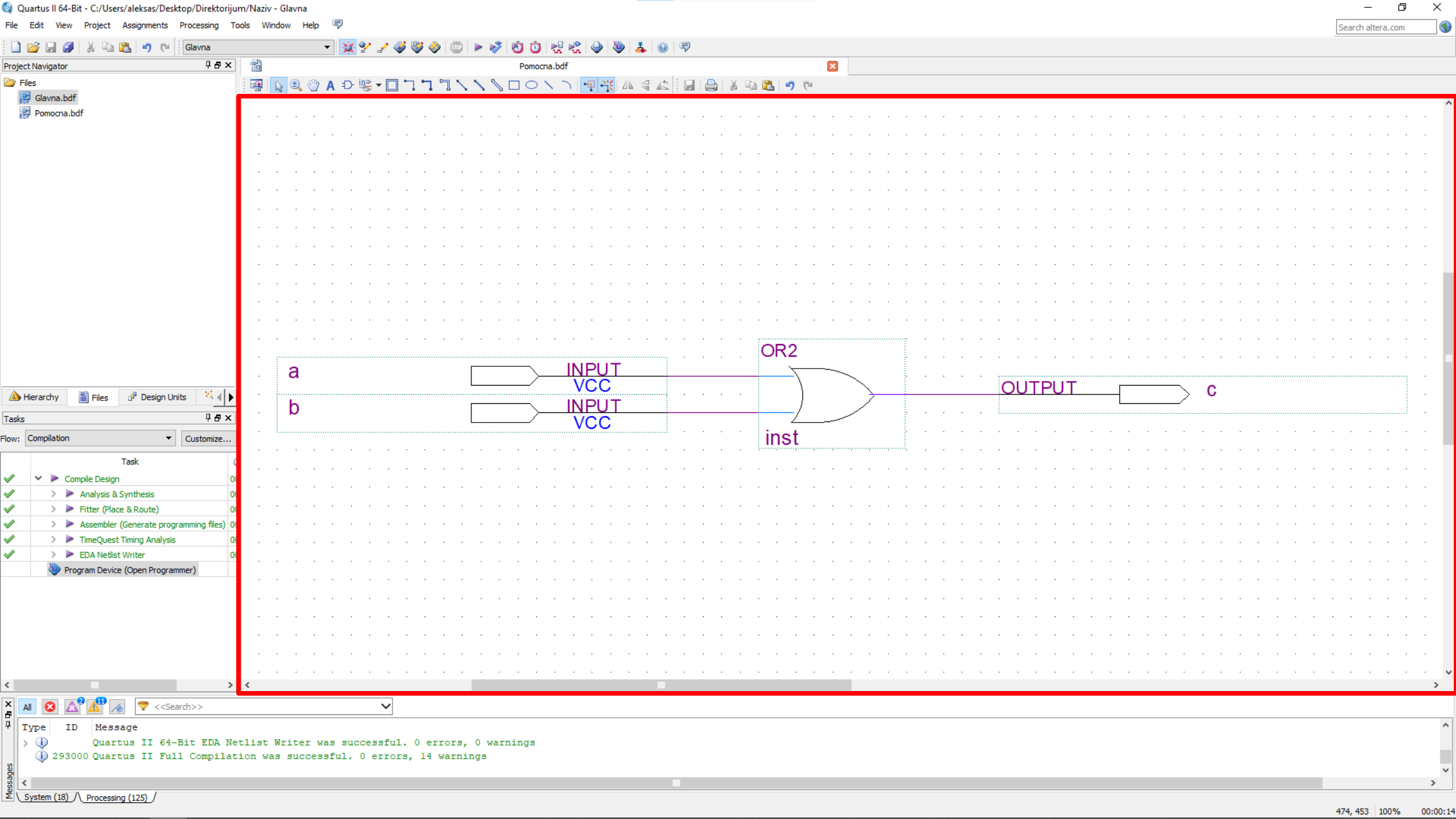
Task	
?	▶ <b>Compile Design</b>
?	> ▶ Analysis & Synthesis 00
?	> ▶ Fitter (Place & Route) 00
?	> ▶ Assembler (Generate programming files) 00
?	> ▶ TimeQuest Timing Analysis 00
?	> ▶ EDA Netlist Writer 00
	▶ Program Device (Open Programmer)

Messages

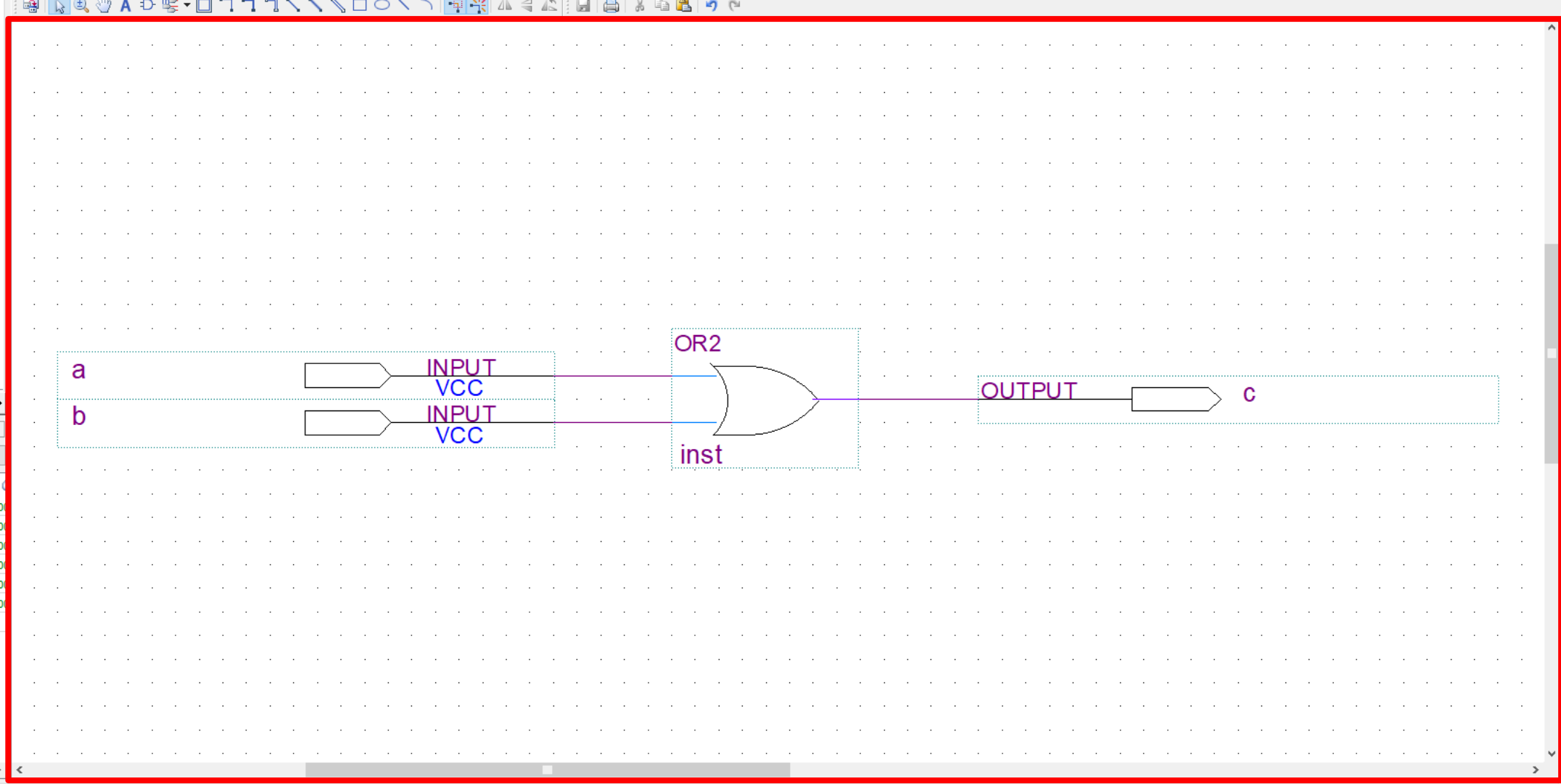
<<Search>>

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 14 warnings

System (18) | Processing (124)



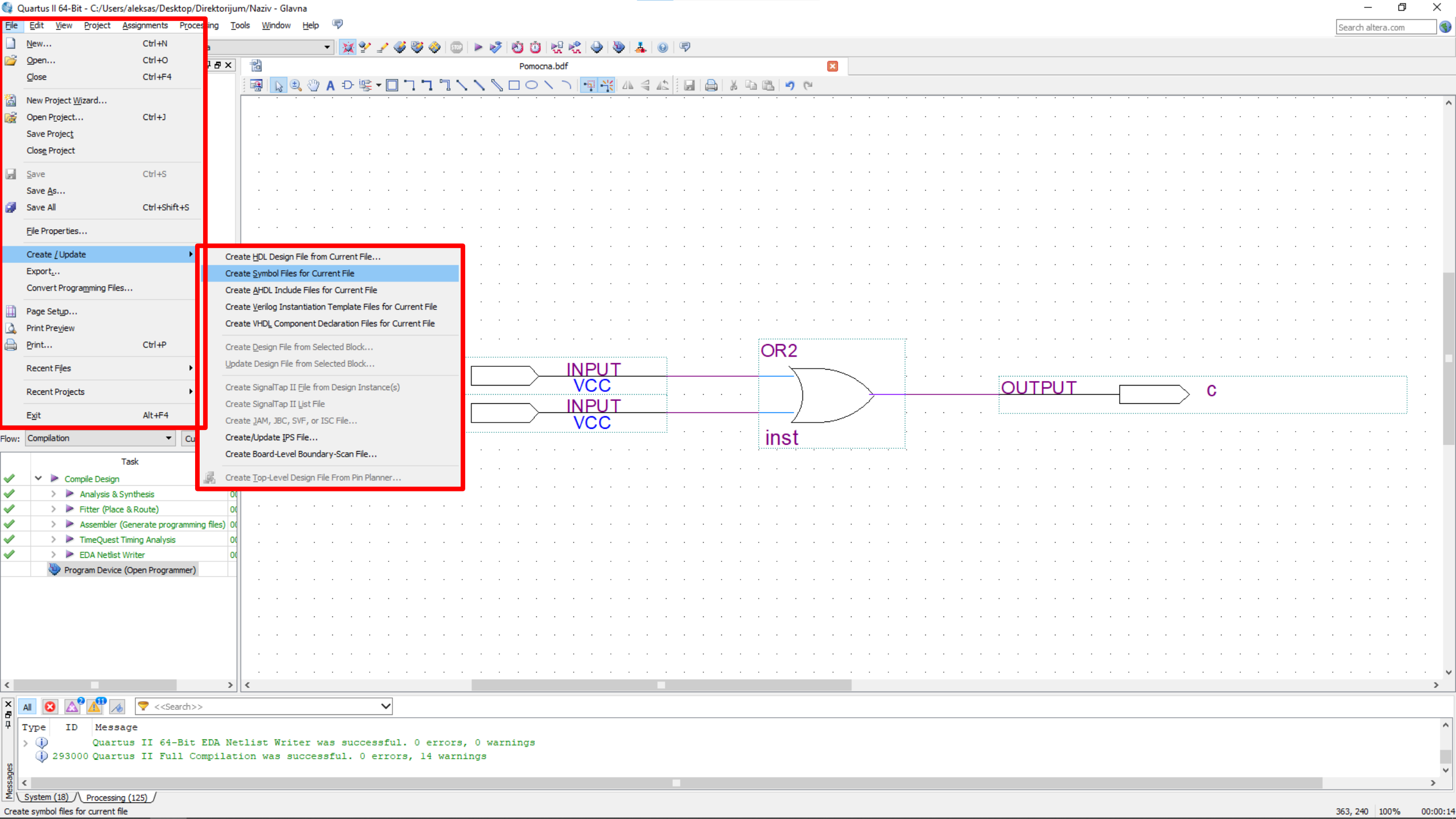
Task	Progress
Compile Design	0%
Analysis & Synthesis	0%
Fitter (Place & Route)	0%
Assembler (Generate programming files)	0%
TimeQuest Timing Analysis	0%
EDA Netlist Writer	0%
Program Device (Open Programmer)	





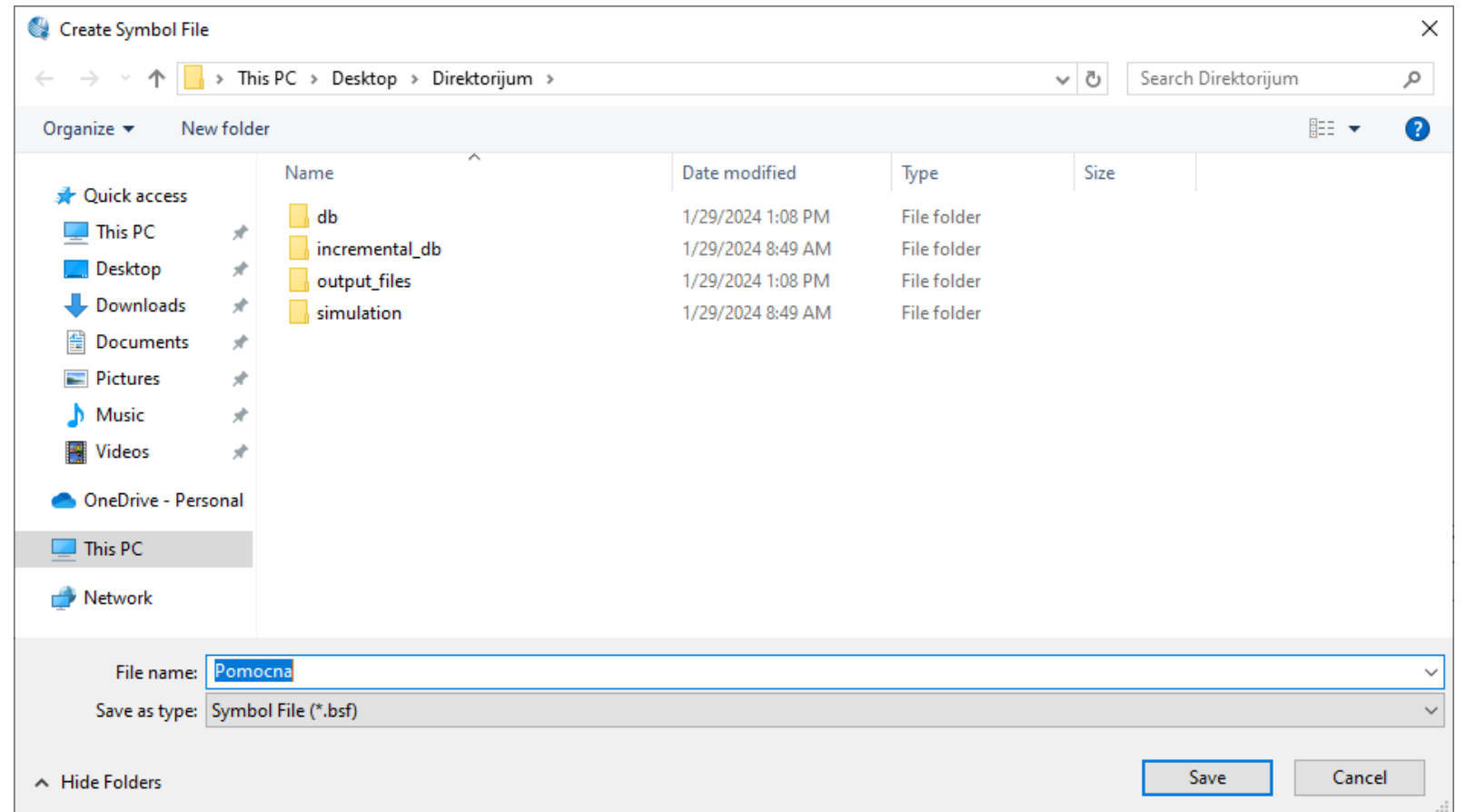
# Прављење симбола

- File -> Create / Update -> Create Symbol Files for Current File
- Save
- OK
- Block Editor -> Symbol Tool
- OK



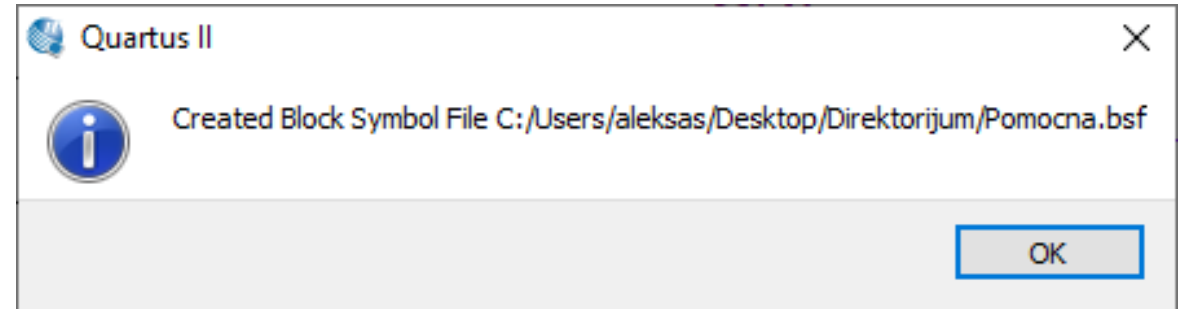
# Прављење симбола

- File -> Create / Update -> Create Symbol Files for Current File
- **Save**
- OK
- Block Editor -> Symbol Tool
- OK



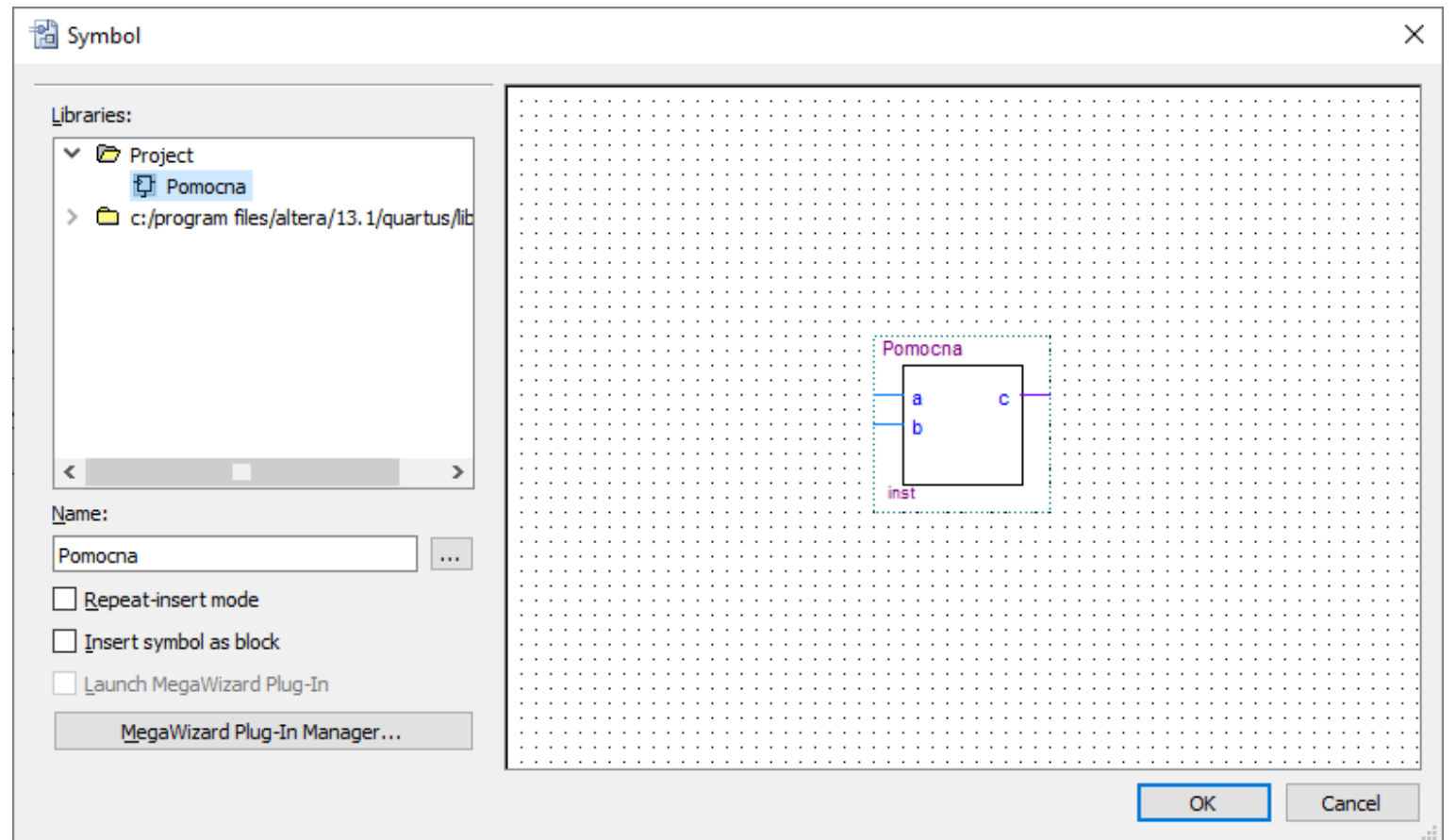
# Прављење симбола

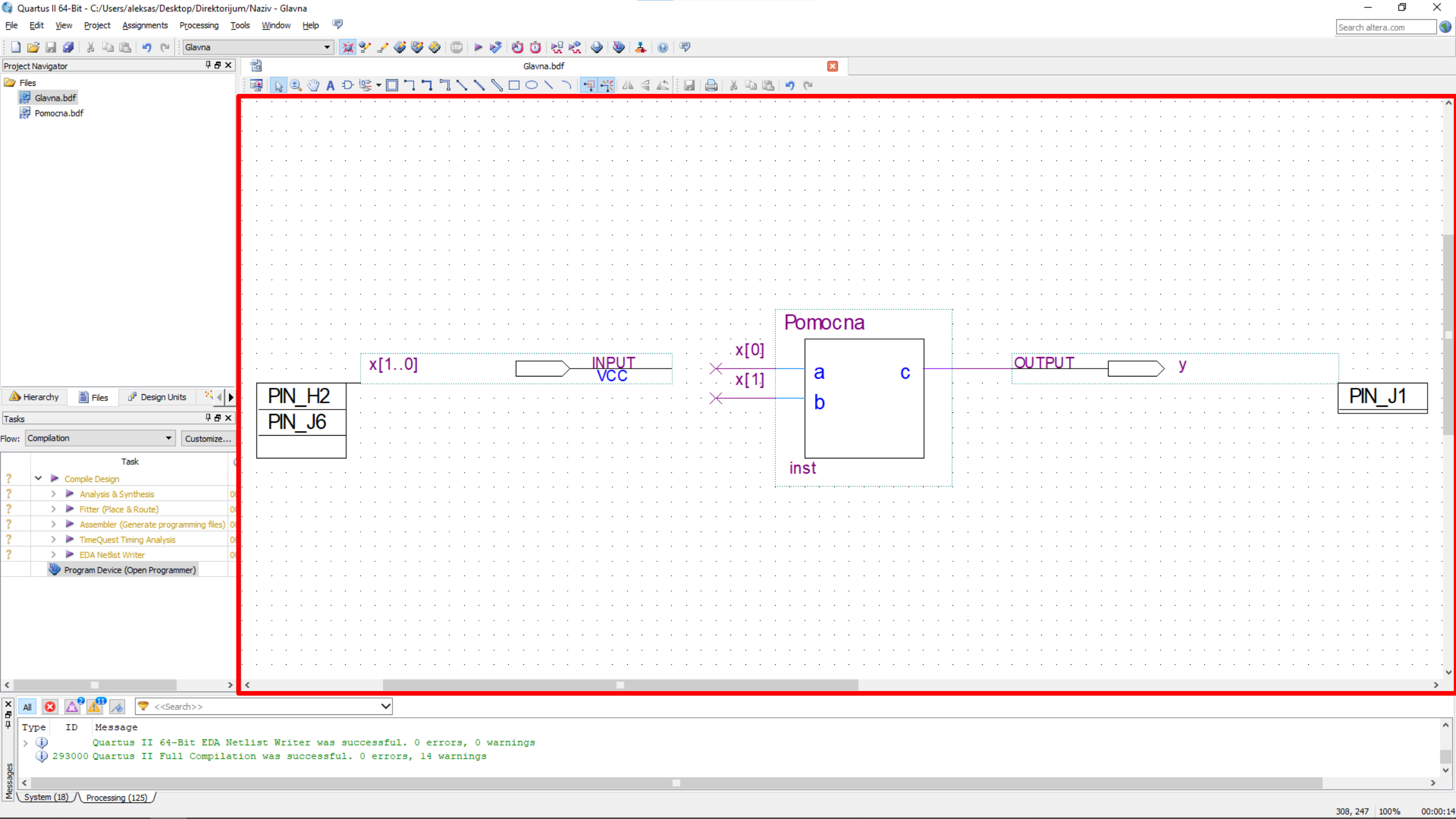
- File -> Create / Update -> Create Symbol Files for Current File
- Save
- **OK**
- Block Editor -> Symbol Tool
- OK

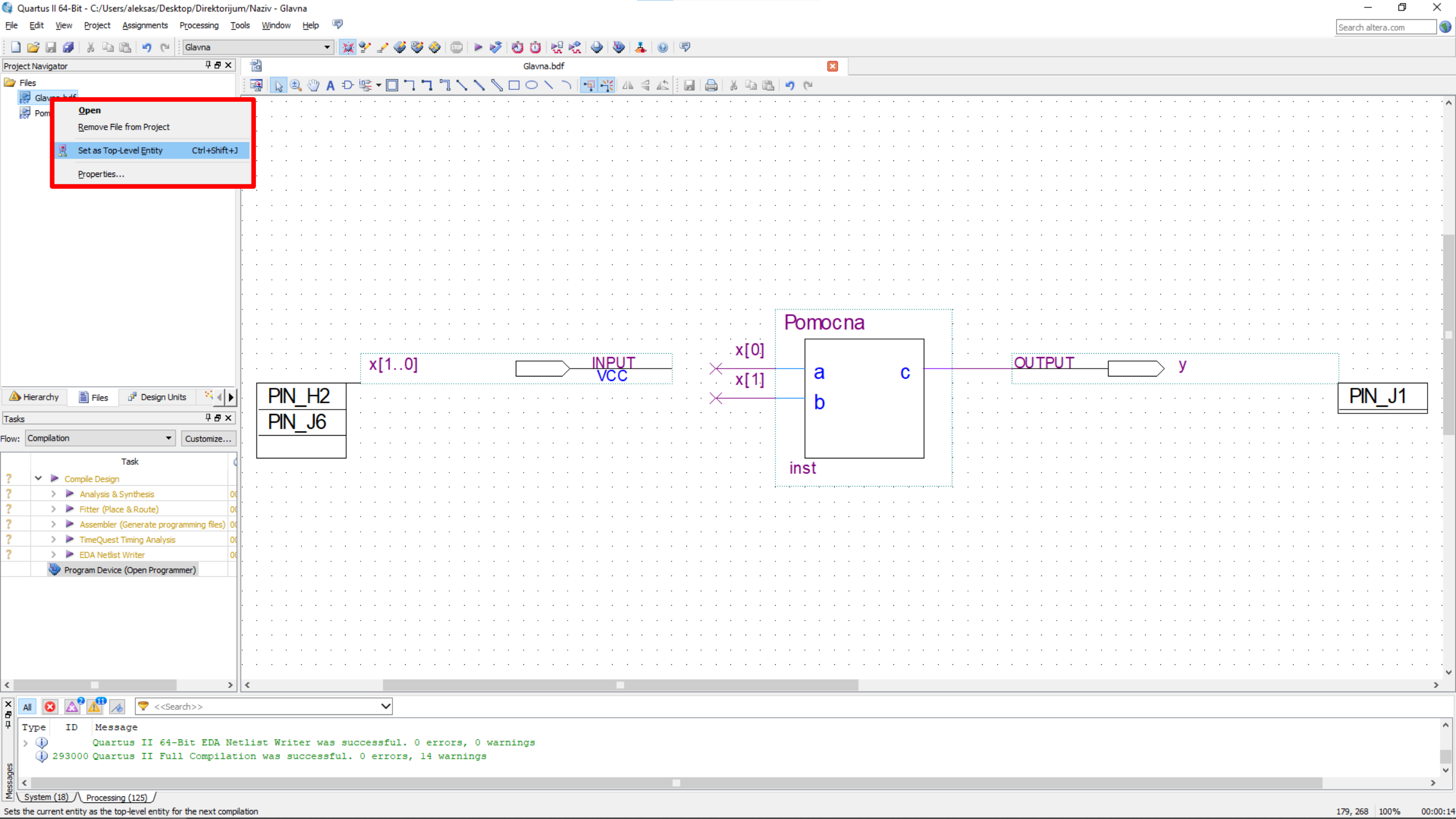


# Прављење симбола

- File -> Create / Update -> Create Symbol Files for Current File
- Save
- OK
- Block Editor -> Symbol Tool
- OK







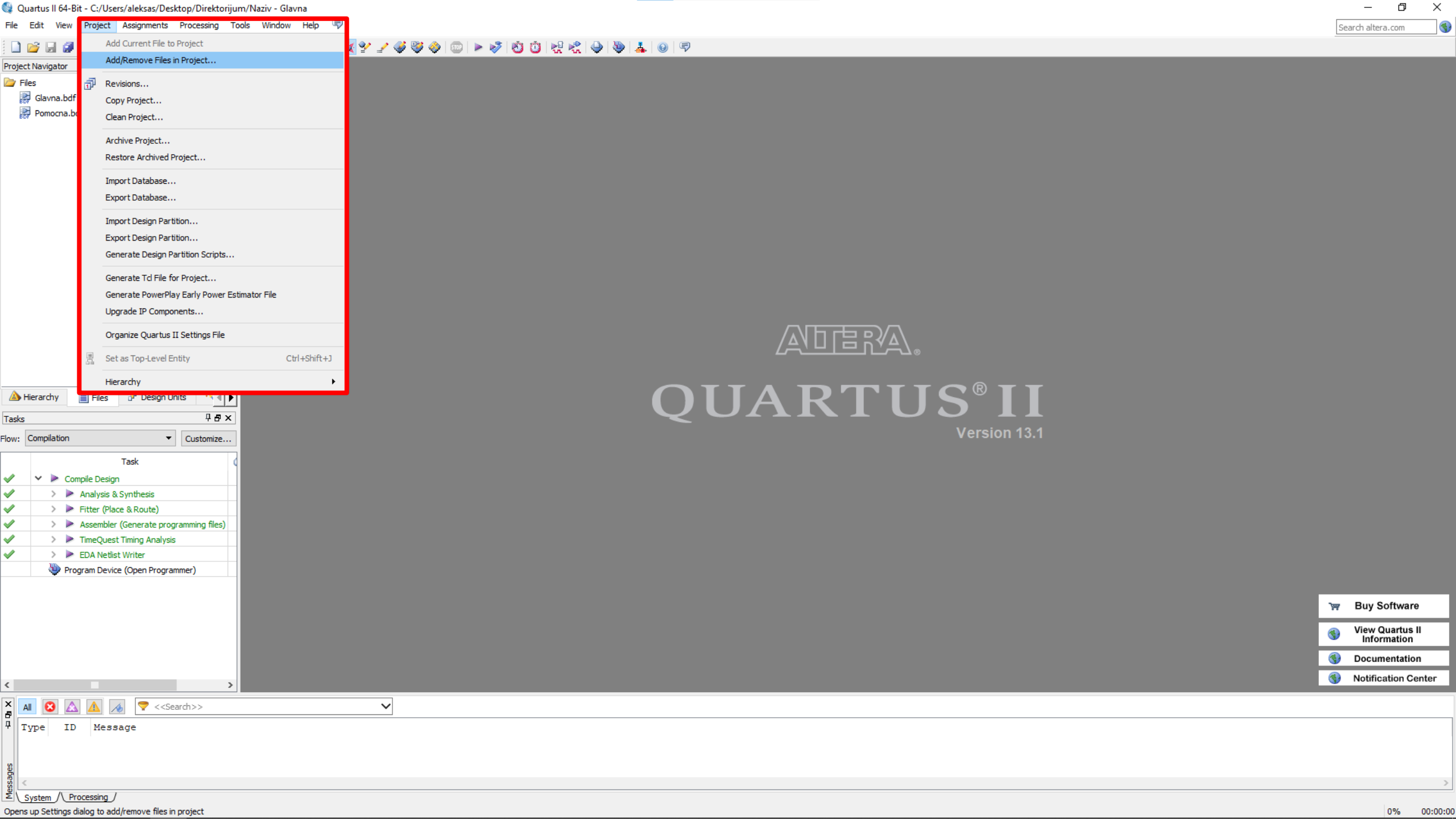
# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project... (Project Navigator -> Files -> Add/Remove Files in Project)
- File Name
- File Name -> Open
- Add All -> Apply -> OK





Name	Date modified	Type	Size
db	1/29/2024 6:34 PM	File folder	
incremental_db	1/29/2024 8:49 AM	File folder	
output_files	1/29/2024 1:16 PM	File folder	
simulation	1/29/2024 8:49 AM	File folder	
Glavna	1/29/2024 1:15 PM	BDF File	3 KB
Glavna.qsf	1/29/2024 1:16 PM	QSF File	4 KB
Glavna.qws	1/29/2024 6:34 PM	QWS File	1 KB
Naziv	1/28/2024 1:06 PM	QPF File	2 KB
Pomocna	1/29/2024 1:08 PM	BDF File	4 KB
Pomocna	1/29/2024 1:12 PM	BSF File	2 KB
Strana	1/29/2024 6:31 PM	BDF File	4 KB
Strana	1/29/2024 6:31 PM	BSF File	2 KB



- Project
  - Assignments
  - Processing
  - Tools
  - Window
  - Help
- Add Current File to Project
  - Add/Remove Files in Project...
  - Revisions...
  - Copy Project...
  - Clean Project...
  - Archive Project...
  - Restore Archived Project...
  - Import Database...
  - Export Database...
  - Import Design Partition...
  - Export Design Partition...
  - Generate Design Partition Scripts...
  - Generate Td File for Project...
  - Generate PowerPlay Early Power Estimator File
  - Upgrade IP Components...
  - Organize Quartus II Settings File
  - Set as Top-Level Entity (Ctrl+Shift+J)
  - Hierarchy

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# QUARTUS® II

Version 13.1

Hierarchy

Files

Design Units

Tasks

Flow: Compilation

Task
✓ Compile Design
✓ > Analysis & Synthesis
✓ > Fitter (Place & Route)
✓ > Assembler (Generate programming files)
✓ > TimeQuest Timing Analysis
✓ > EDA Netlist Writer
Program Device (Open Programmer)

- [Buy Software](#)
- [View Quartus II Information](#)
- [Documentation](#)
- [Notification Center](#)

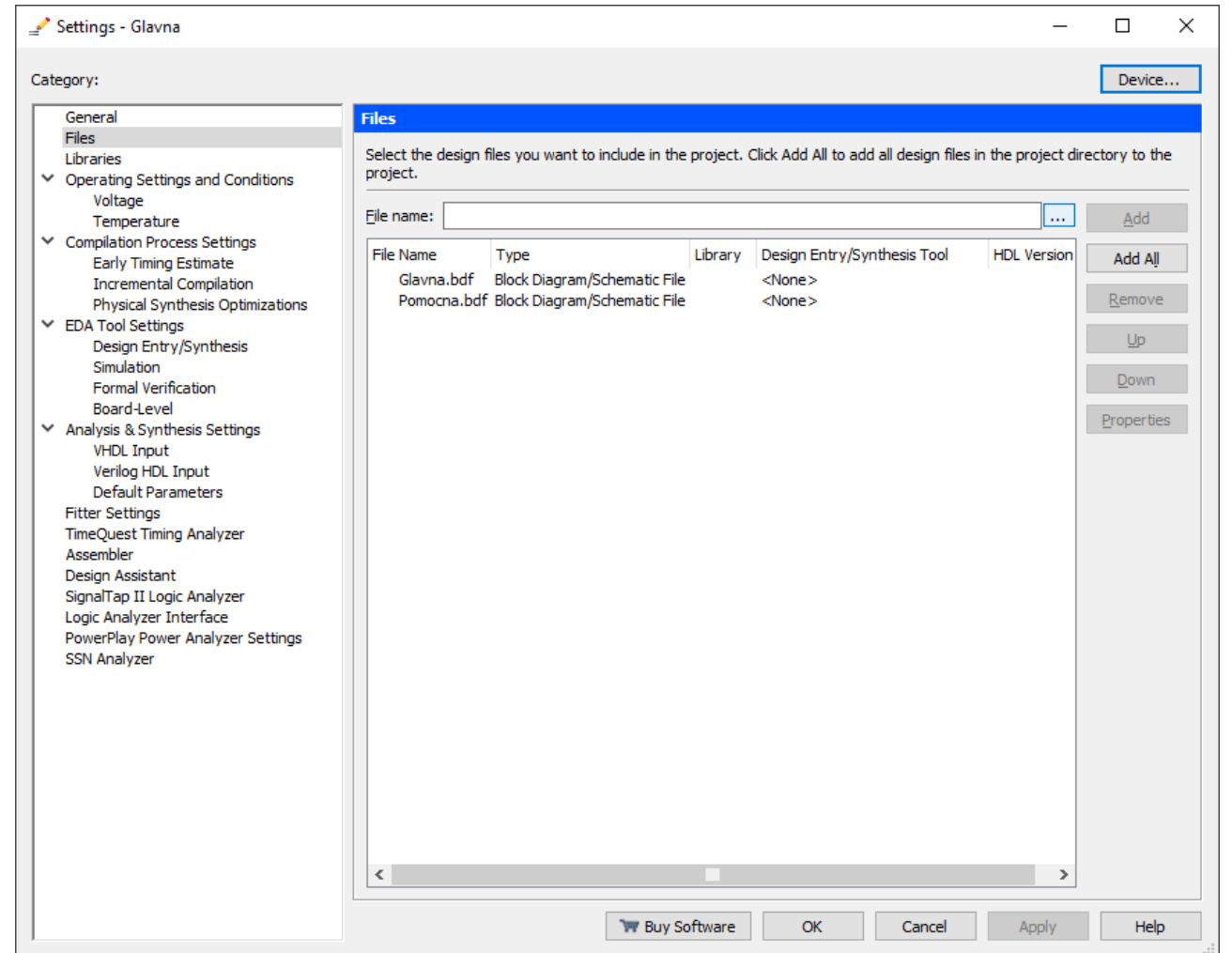
Messages

System / Processing

Type	ID	Message
		Opens up Settings dialog to add/remove files in project

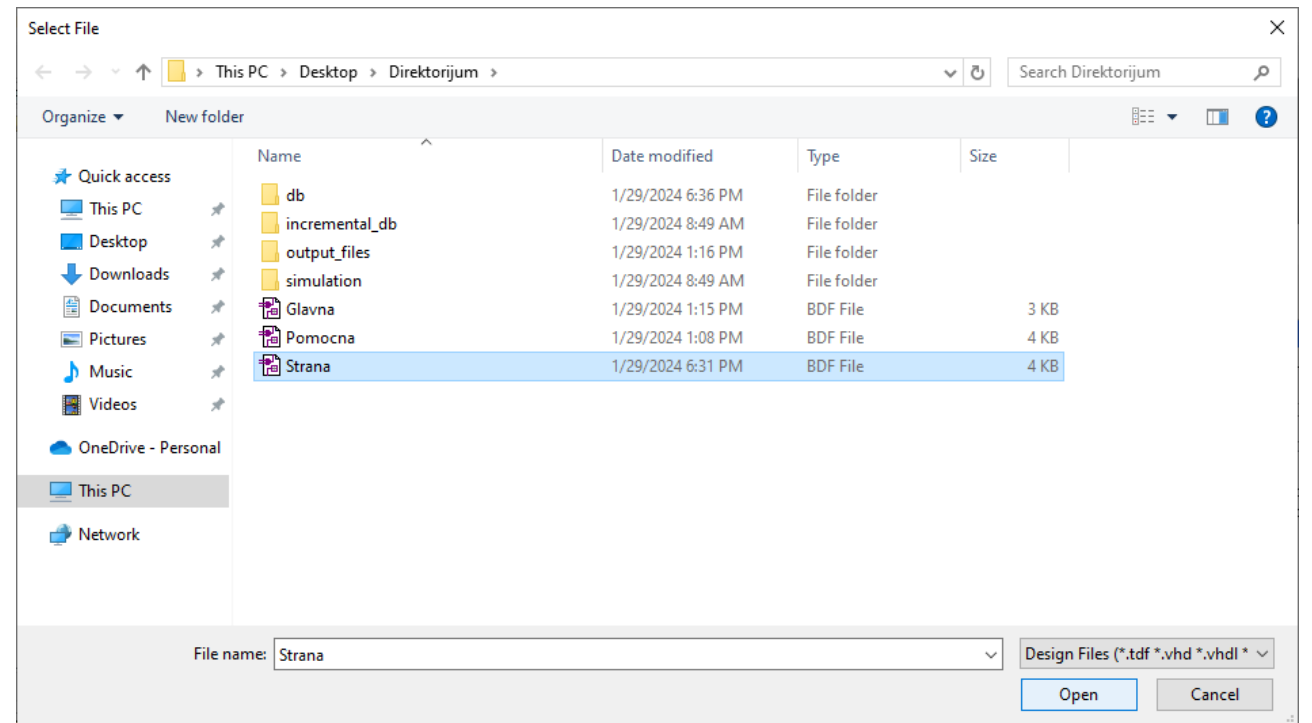
# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project...  
(Project Navigator -> Files -> Add/Remove Files in Project)
- **File Name**
- File Name -> Open
- Add All -> Apply -> OK



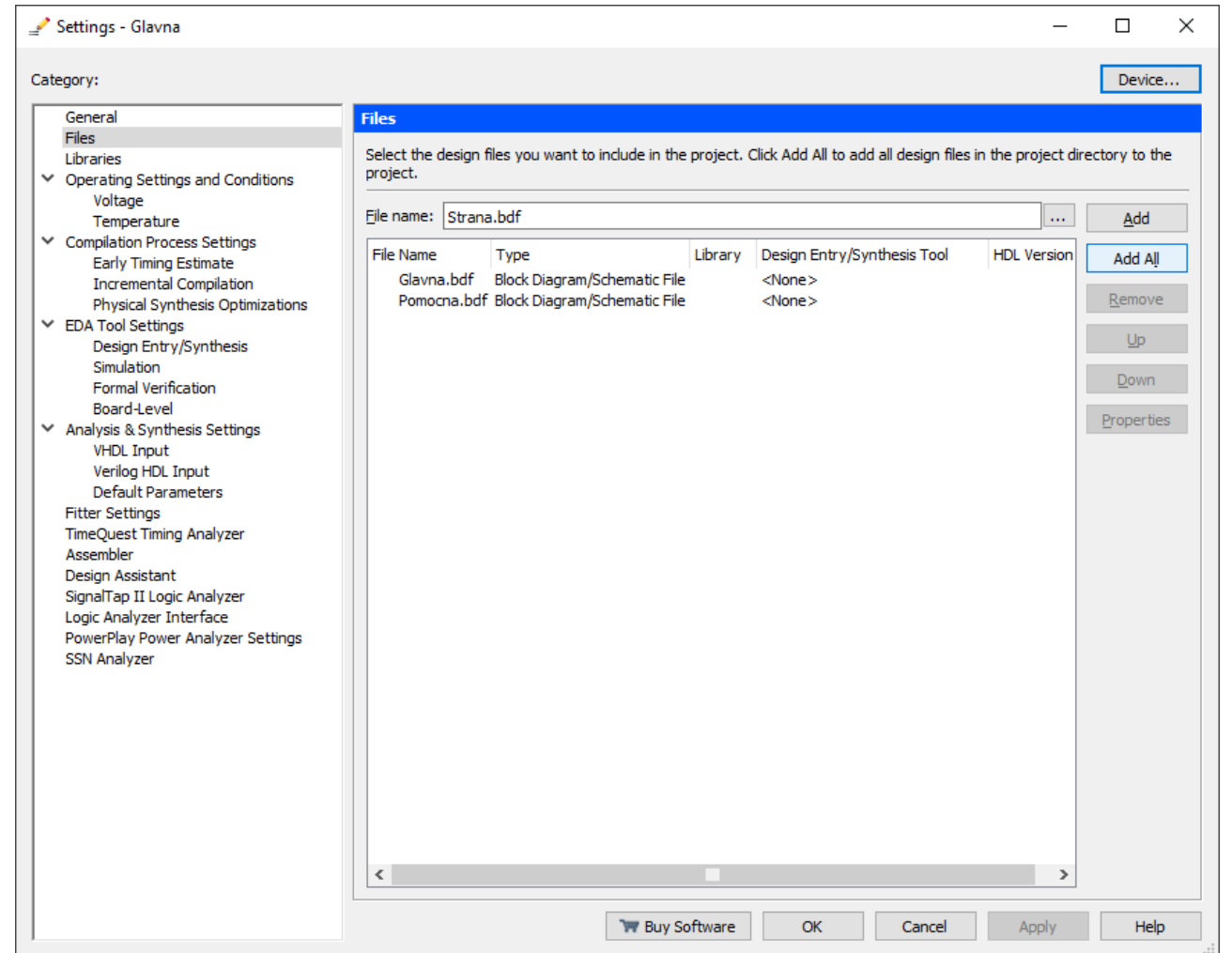
# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project... (Project Navigator -> Files -> Add/Remove Files in Project)
- File Name
- **File Name -> Open**
- Add All -> Apply -> OK



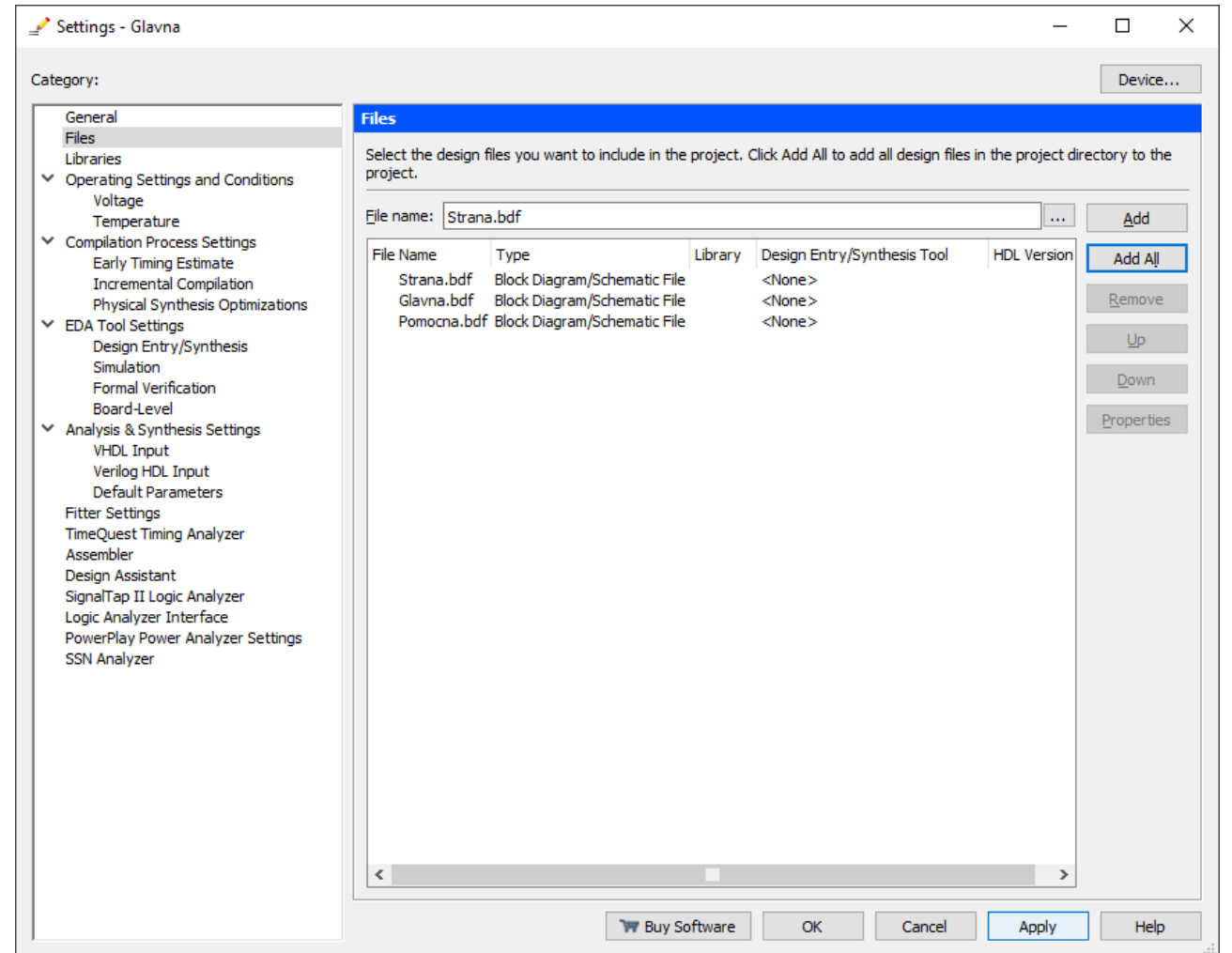
# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project...  
(Project Navigator -> Files -> Add/Remove Files in Project)
- File Name
- File Name -> Open
- **Add All -> Apply -> OK**



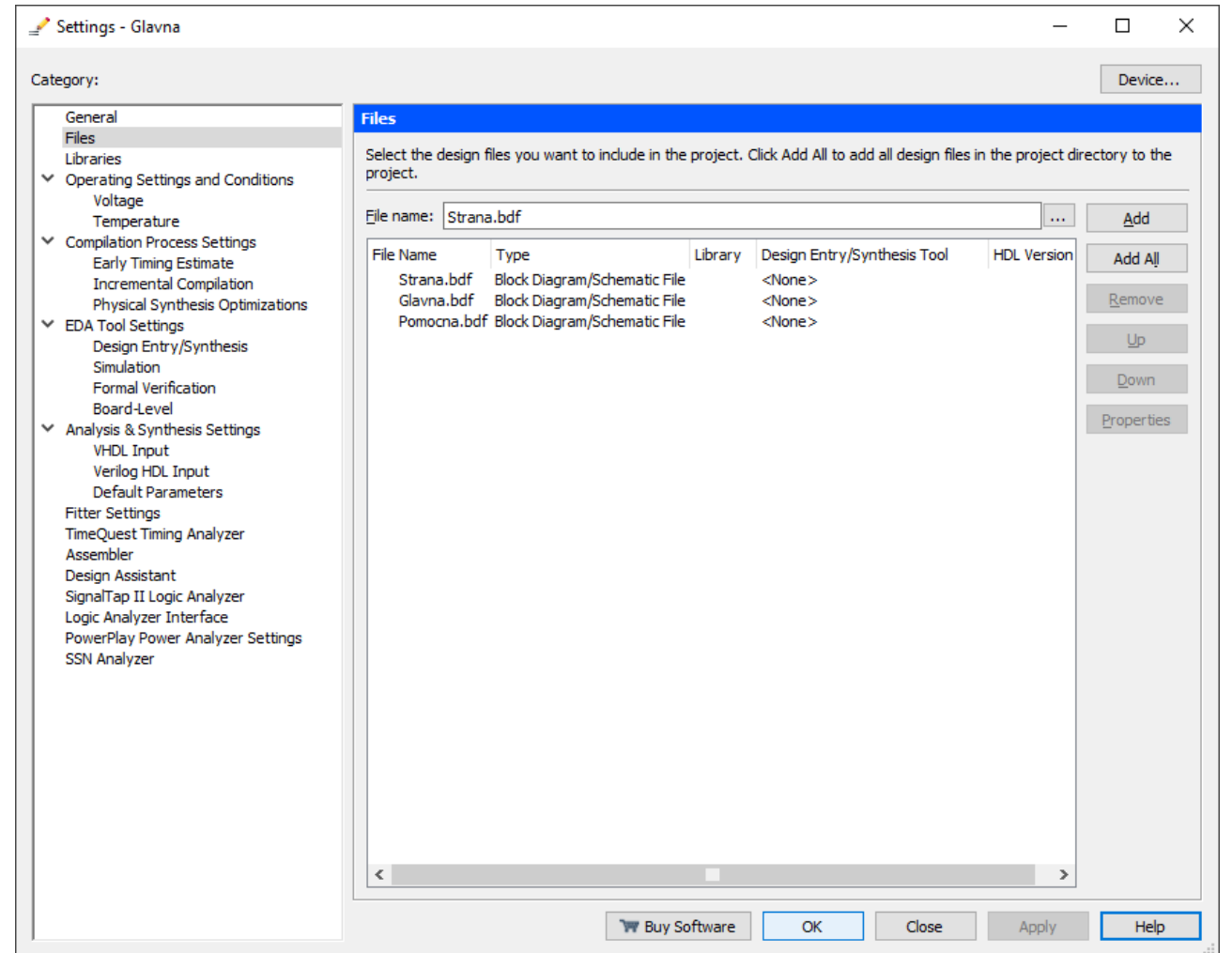
# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project...  
(Project Navigator -> Files -> Add/Remove Files in Project)
- File Name
- File Name -> Open
- **Add All -> Apply -> OK**



# Додавање фајлова у пројекат

- Copy
- Paste
- Project -> Add/Remove Files in Project...  
(Project Navigator -> Files -> Add/Remove Files in Project)
- File Name
- File Name -> Open
- **Add All -> Apply -> OK**





Glavna

Project Navigator

Files

- Glavna.bdf
- Pomocna.bdf
- Strana.bdf

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

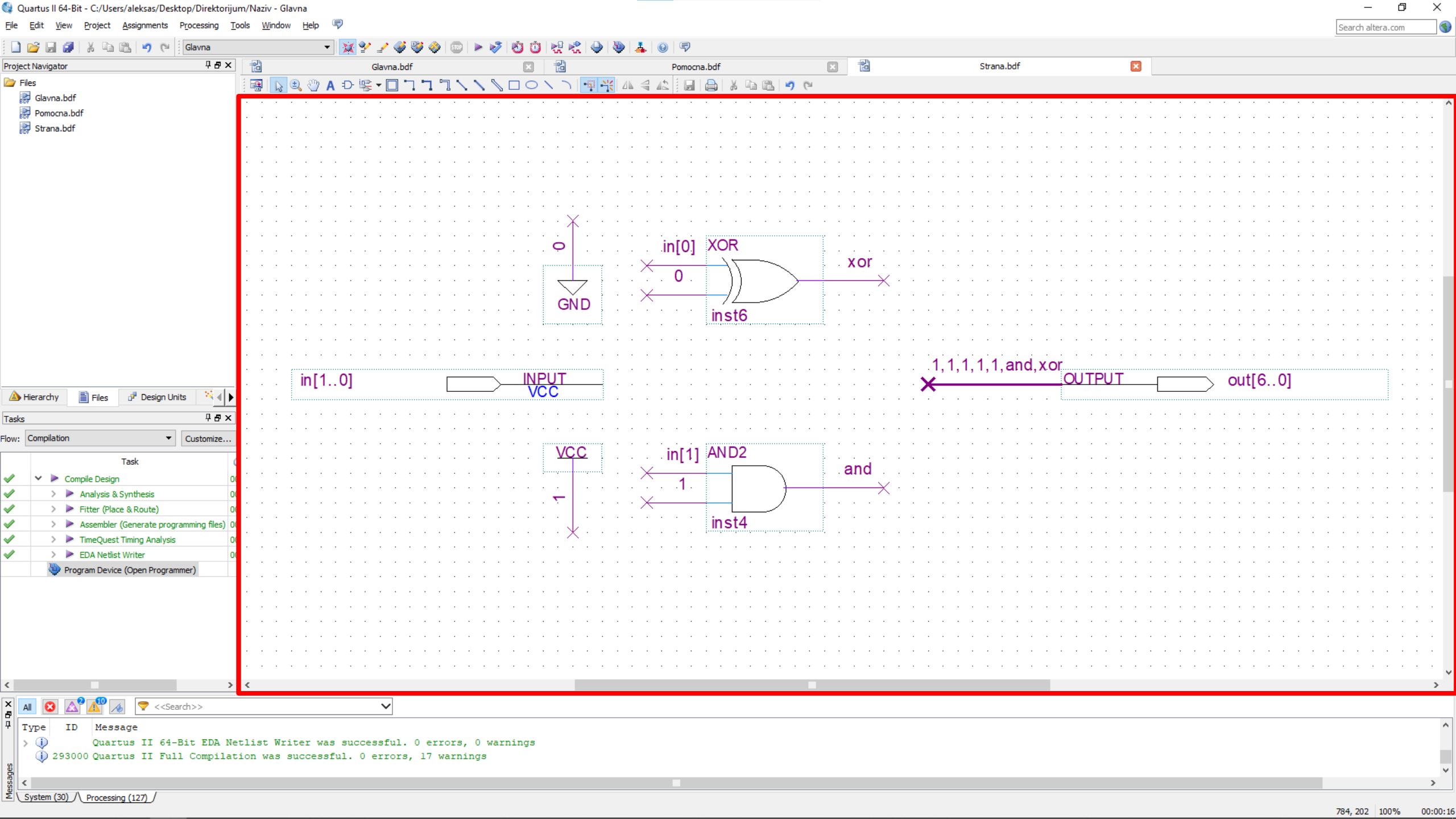
	Task	
✓	▶ Compile Design	00
✓	> ▶ Analysis & Synthesis	00
✓	> ▶ Fitter (Place & Route)	00
✓	> ▶ Assembler (Generate programming files)	00
✓	> ▶ TimeQuest Timing Analysis	00
✓	> ▶ EDA Netlist Writer	00
	▶ Program Device (Open Programmer)	

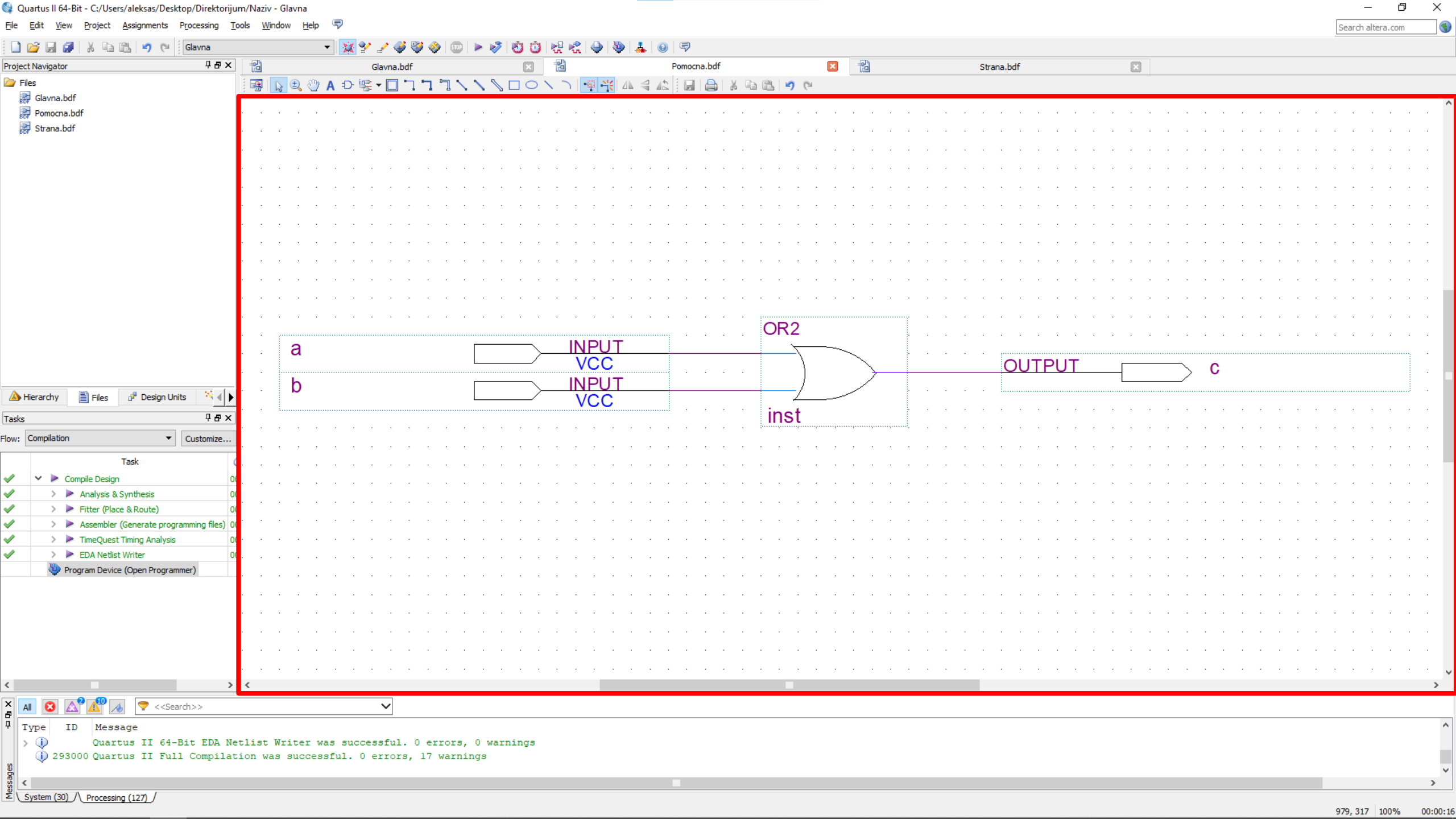
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Version 13.1

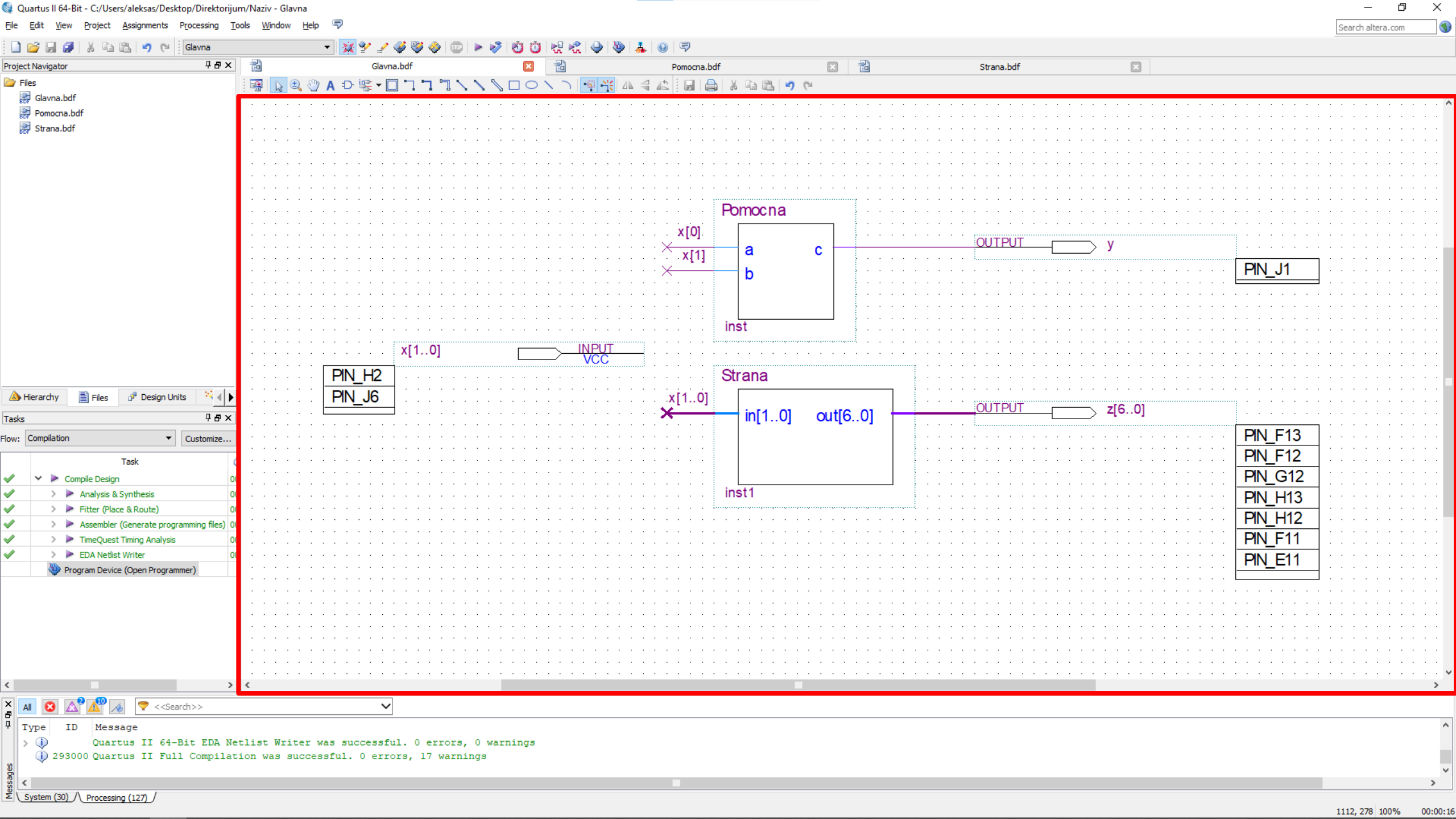
[Buy Software](#)[View Quartus II Information](#)[Documentation](#)[Notification Center](#)

All &lt;&lt;Search&gt;&gt;

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 17 warnings

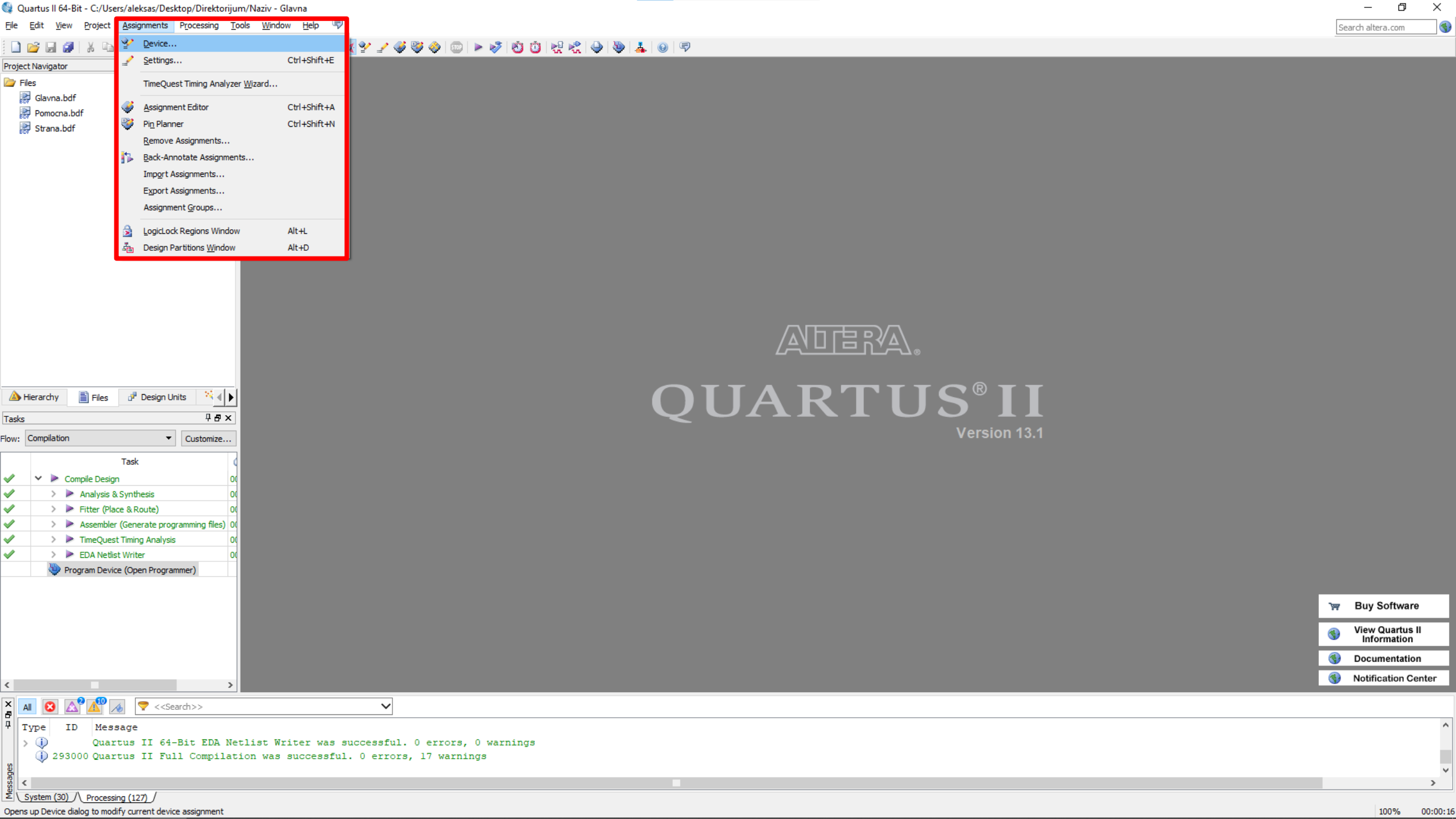






# Промена плочице

- Assignments -> Device...
- Family
- Yes
- Name filter
- Yes
- OK



File Edit View Project Assignments Processing Tools Window Help

- Device...
- Settings... Ctrl+Shift+E
- TimeQuest Timing Analyzer Wizard...
- Assignment Editor Ctrl+Shift+A
- Pin Planner Ctrl+Shift+N
- Remove Assignments...
- Back-Annotate Assignments...
- Import Assignments...
- Export Assignments...
- Assignment Groups...
- LogicLock Regions Window Alt+L
- Design Partitions Window Alt+D

Project Navigator

Files

- Glavna.bdf
- Pomocna.bdf
- Strana.bdf

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# QUARTUS® II

Version 13.1

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Progress
Compile Design	00
> Analysis & Synthesis	00
> Fitter (Place & Route)	00
> Assembler (Generate programming files)	00
> TimeQuest Timing Analysis	00
> EDA Netlist Writer	00
Program Device (Open Programmer)	

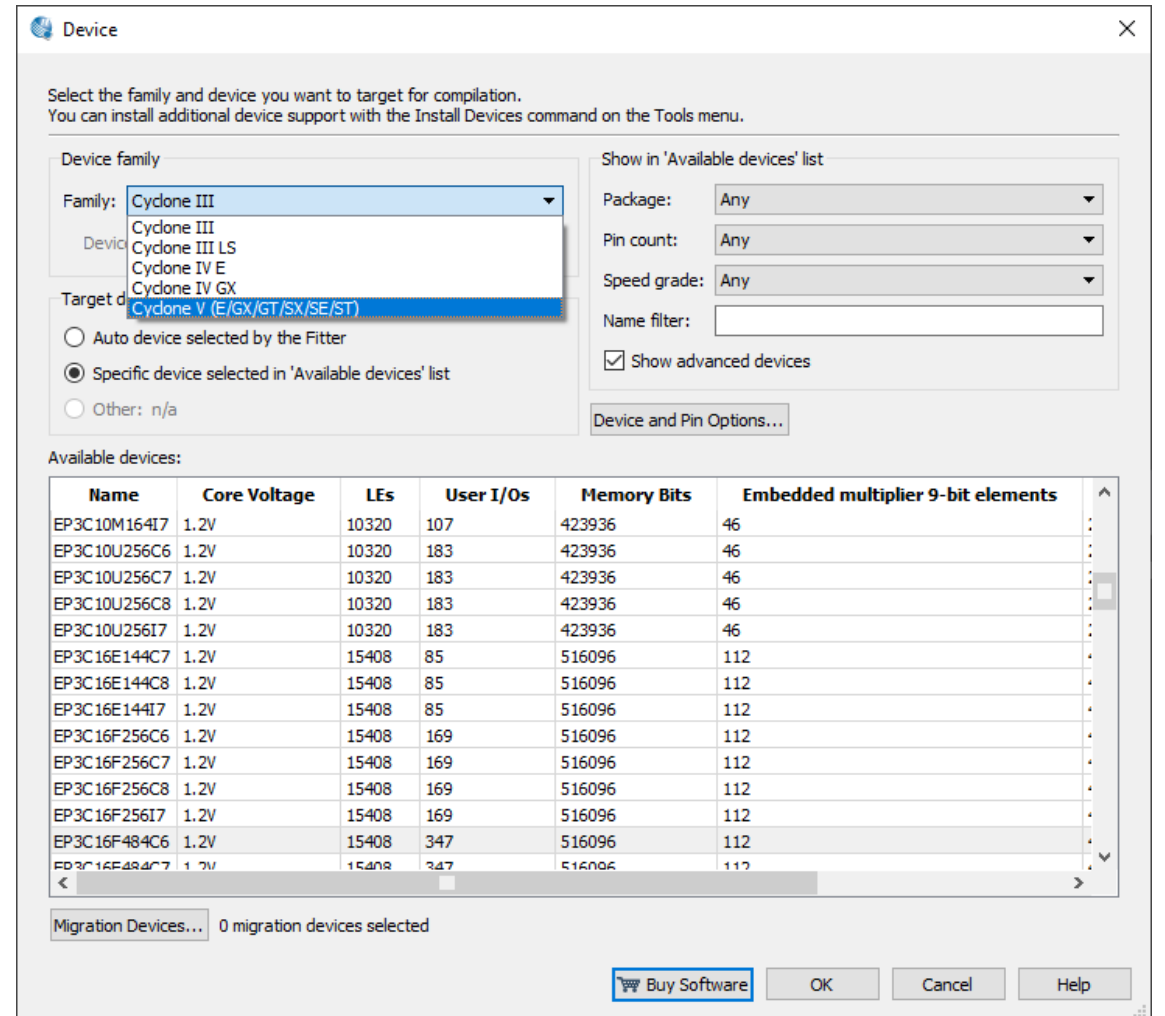
- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

All <<Search>>

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 17 warnings

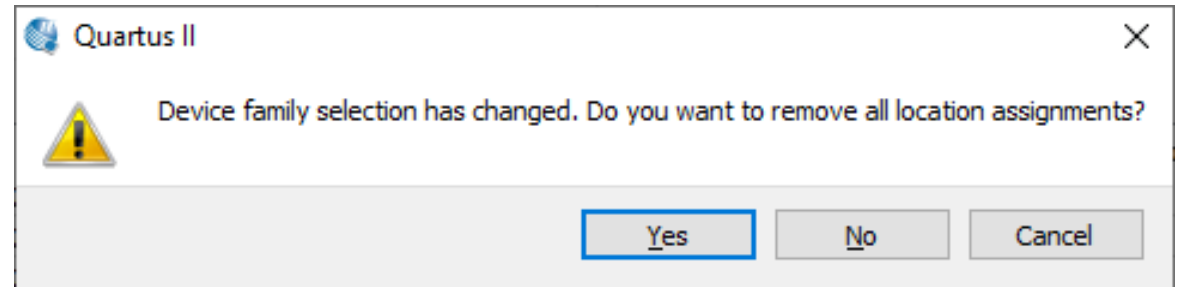
# Промена плочице

- Assignments -> Device...
- **Family**
- Yes
- Name filter
- Yes
- OK



# Промена плочице

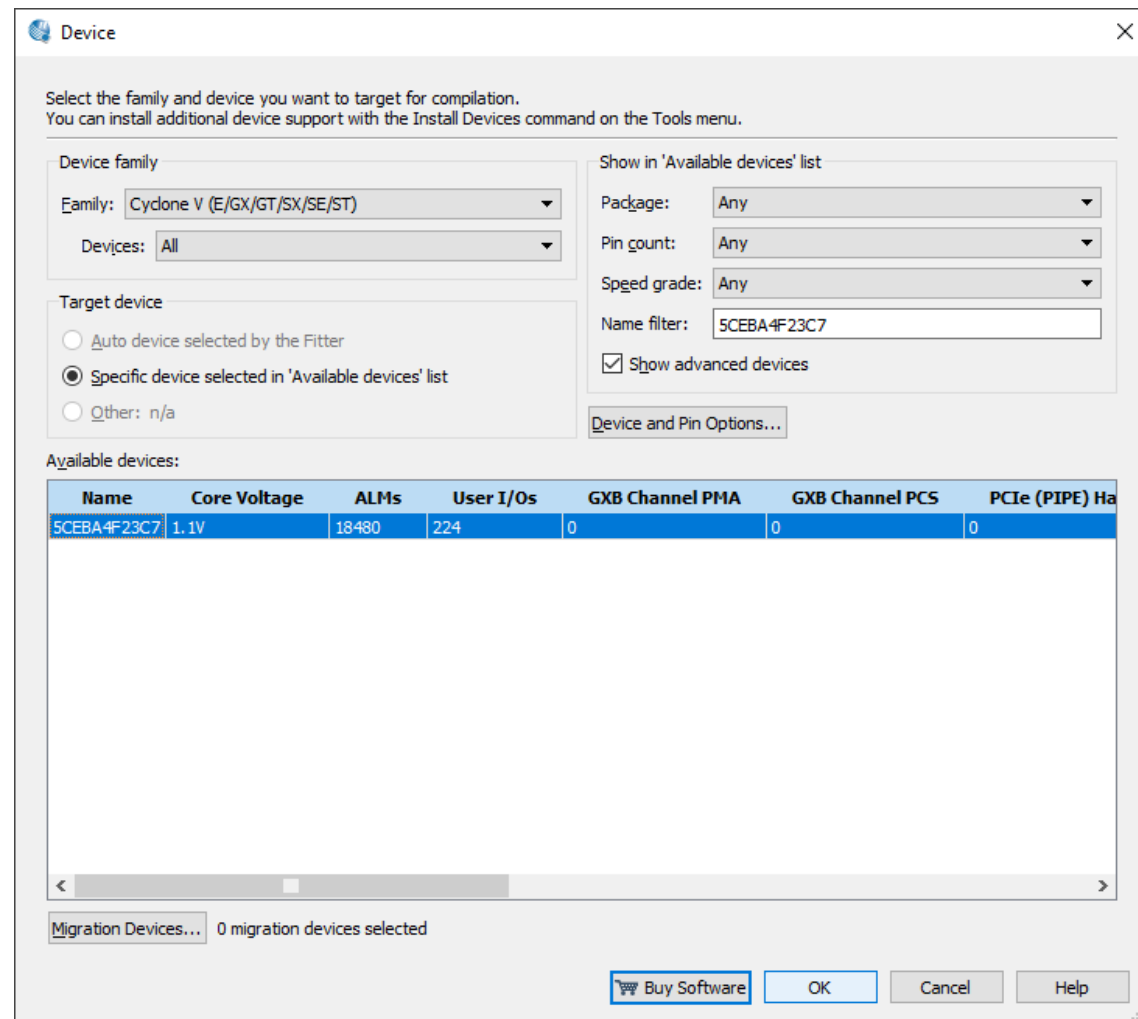
- Assignments -> Device...
- Family
- **Yes**
- Name filter
- Yes
- OK





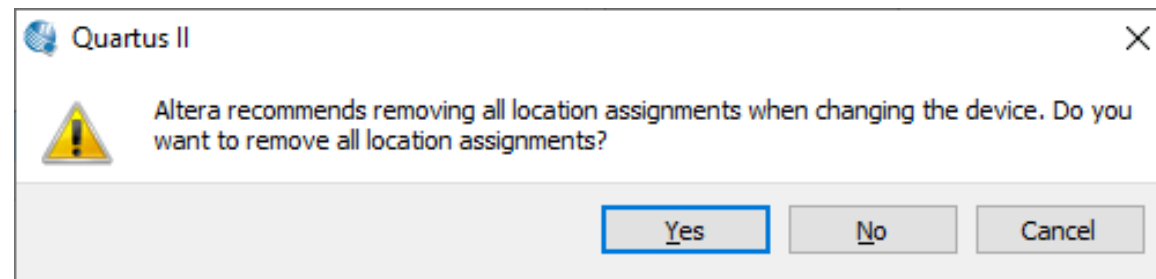
# Промена плочице

- Assignments -> Device...
- Family
- Yes
- **Name filter**
- Yes
- OK



# Промена плочице

- Assignments -> Device...
- Family
- Yes
- Name filter
- **Yes**
- OK



# Чишћење пројекта

- Project -> Clean Project...
- Revision Name -> OK

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

- Files
  - Glavna.bdf
  - Pomocna.bdf
  - Strana.bdf

Project Menu:

- Add Current File to Project
- Add/Remove Files in Project...
- Revisions...
- Copy Project...
- Clean Project...**
- Archive Project...
- Restore Archived Project...
- Import Database...
- Export Database...
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- Upgrade IP Components...
- Organize Quartus II Settings File
- Set as Top-Level Entity Ctrl+Shift+J
- Hierarchy

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Hierarchy

Tasks

Flow: Compilation Customize...

Task	Progress
Compile Design	00
> Analysis & Synthesis	00
> Fitter (Place & Route)	00
> Assembler (Generate programming files)	00
> TimeQuest Timing Analysis	00
> EDA Netlist Writer	00
Program Device (Open Programmer)	

- Buy Software
- View Quartus II Information
- Documentation
- Notification Center

All <<Search>>

Messages

Type	ID	Message
>		Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 17 warnings

System (30) / Processing (127)

# Чишћење пројекта

- Project -> Clean Project...
- Revision Name -> OK

